

# DB13 DIS Schematics Document

**Sandy Bridge  
Intel PCH**

**2010-11-25**

**REV : X00**

*DY :None Installed*

*PSL: KBC795 PSL circuit for 10mW solution installed.*

*10mW: External circuit for 10mW solution installed.*

*GSENSOR\_ST: Stuff for ST G-Sensor*

*GSENSOR\_ADI: Stuff for ADI G-Sensor*

<Core Design>



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Title

**Cover**

Size  
A3

Document Number

**DB13 DIS**

Rev  
**X00**

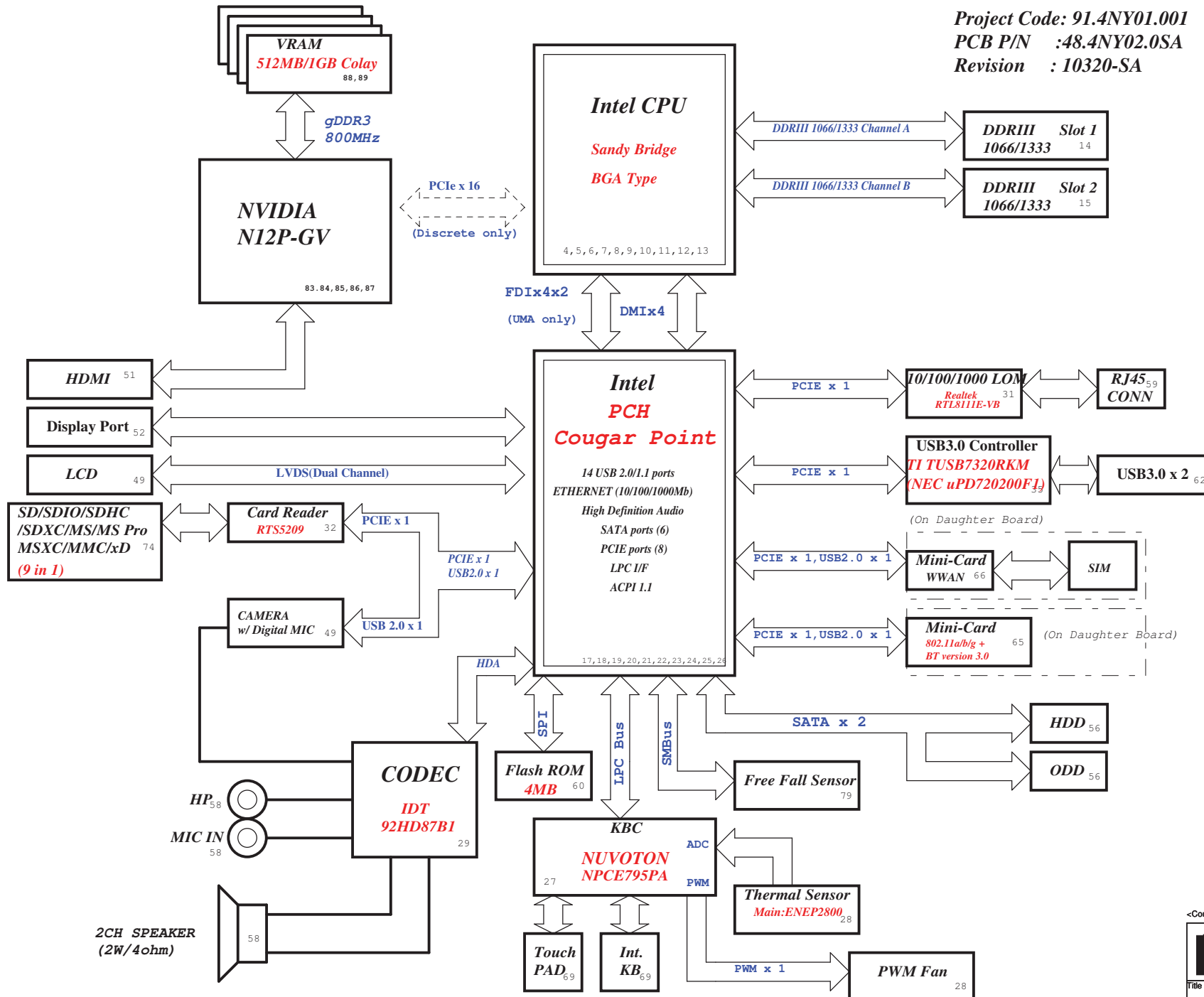
Date: Friday, November 26, 2010

Sheet 1 of 105

# DB13 DIS Block Diagram

##OnMainBoard

Project Code: 91.4NY01.001  
PCB P/N :48.4NY02.0SA  
Revision : 10320-SA



CPU DC/DC	
VT1316+VT1317	42
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
VT1316+VT1317	44
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE
SYSTEM DC/DC	
TPS51461	48
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0
SYSTEM DC/DC	
VT358	46
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3
SYSTEM DC/DC	
VT357	45
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
TI CHARGER	
BQ24745	40
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT
SYSTEM DC/DC	
TPS51427	41
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5
SYSTEM DC/DC	
TPS51311	47
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0
Switches	
36	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0
PCB LAYER	
DIS	
L1:Top L2:GND L3:Signal L4:Signal L5:VCC L6:Signal L7:GND L8:Bottom	

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Block Diagram		
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PCH Strapping Huron River Schematic Checklist Rev.1\_0

Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> <b>Default Mode:</b> Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Enable when Pull-up.
INIT3_3V#	Weak internal pull-up. This signal should not be pulled low. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
INTVRMEN	<b>Integrated 1.05 V VRM Enable / Disable</b> Integrated 1.05 V VRMs is enabled when high. This signal should always be pulled high
DF_TVS	<b>DMI and FDI Tx/Rx Termination Voltage</b> Weak internal pull-down. It needs to be connected to PROC_SELECT with a 1K±5% pull-up resistor to PCH VCCPNAND rail and a 4.7K±5% series resistor.
SATA1GP /GPIO19	<b>Boot BIOS Strap bit 0</b> This Signal has a weak internal pull-up. Note: This field determines the destination of accesses to the BIOS memory range. This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC
HDA_SDO	Signal has a weak internal pull-down. Default: the security measures defined in the Flash Descriptor will be in effect. Pull-up: the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing or debug environments ONLY.
HDA_SYNC	<b>On-Die PLL Voltage Regulator Voltage Select</b> This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low. Needs to be pulled High for Huron River platform.
GPIO15	<b>TLS Confidentiality</b> Low - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: A strong pull-up may be needed for GPIO functionality
DSWVRMEN	<b>Deep S4/S5 Well On-Die Voltage Regulator Enable</b> This signal enables the internal Deep Sleep 1.05 V regulators. This signal must be always pulled-up to VccRTC.
GPIO28	<b>On-Die PLL Voltage Regulator</b> This signal has a weak internal pull-up. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled. If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail.

PCIE Routing

LANE1	X
LANE2	LAN (I/O Board)
LANE3	Mini Card2(WWAN)
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Card Reader
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	N/A
2	N/A
3	N/A
4	ODD
5	N/A

USB Table

Pair	Device
0	X
1	X
2	X
3	X
4	Mini Card2 (WWAN)
5	X
6	X
7	X
8	X
9	X
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

Processor Strapping Huron River Schematic Checklist Rev.1\_0

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	<b>PCI-Express Static Lane Reversal</b>	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	0
CFG[4]	<b>Display Port Presence strap</b>	1: Disabled - No Physical Display Port attached to Embedded Display Port. 0: Enabled - An external Display Port device is connectd to the Embedded Display Port	1
CFG[6:5]	<b>PCI-Express Port Bifurcation Straps</b>	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	<b>PEG DEFER TRAINING</b>	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I <sup>2</sup> C / SMBus Addresses		Ref Des	HURON RIVER ORB		
Device			Address	Hex	Bus
EC SMBus 1 Battery Capacity Board					KBC_SDA1/KBC_SCL1 KBC_SDA1/KBC_SCL1
EC SMBus 2 PCH MXM LCD Thermal Sensor					KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2
PCH SMBus CK505 Clock Generator SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot					PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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Title			
<b>Table of Content</b>			
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Note:  
Intel DMI supports both Lane  
Reversal and polarity inversion  
but only at PCH side. This is  
enabled via a soft strap.

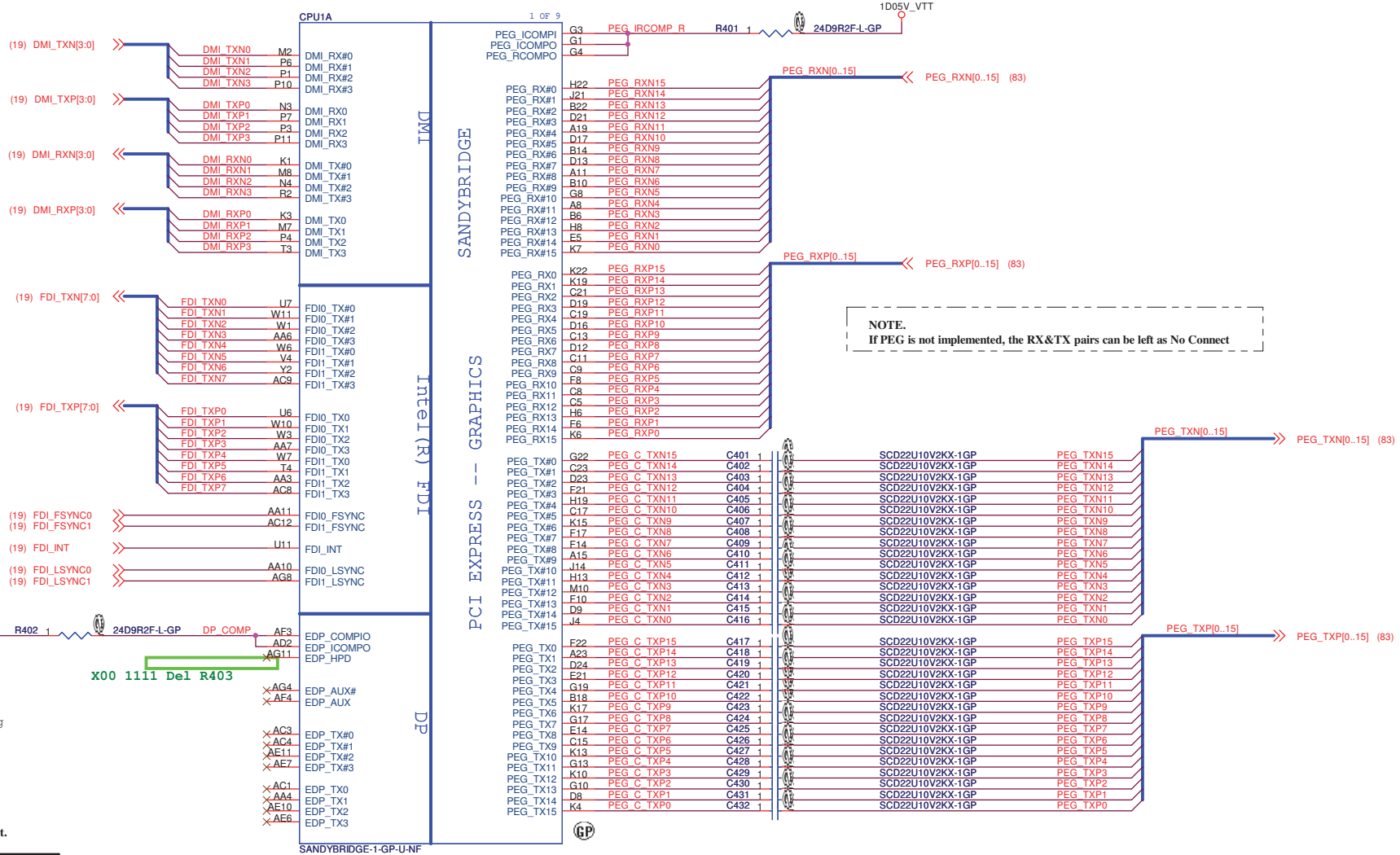
Note:  
Intel FDI supports both Lane  
Reversal and polarity inversion  
but only at PCH side. This is  
enabled via a soft strap.

Note:  
Lane reversal does not apply to  
FDI sideband signals.

Signal Routing Guideline:  
EDP\_ICOMPO keep W/S=12/15 mils and routing  
length less than 500 mils.  
EDP\_COMPIO keep W/S=4/15 mils and routing  
length less than 500 mils.

NOTE.  
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

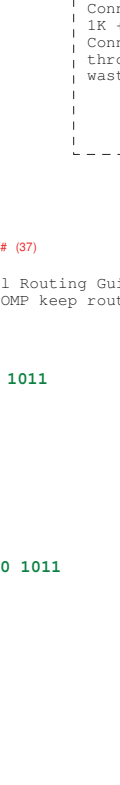
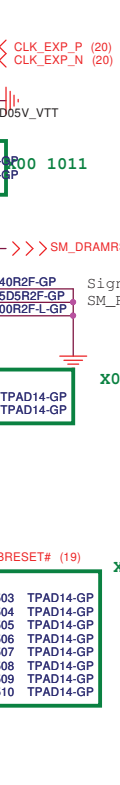
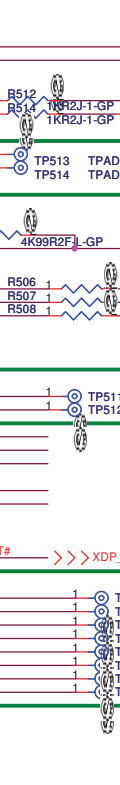
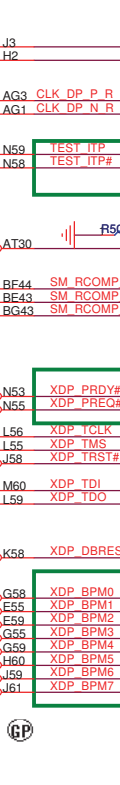
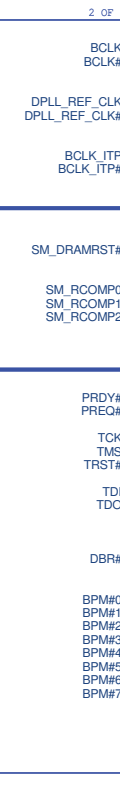
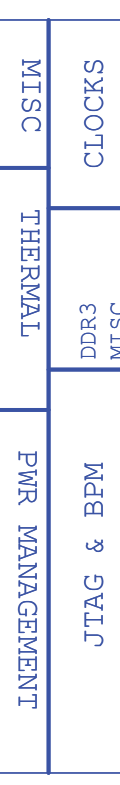
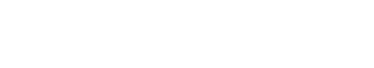
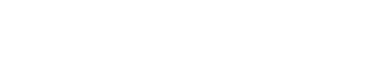
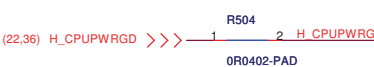
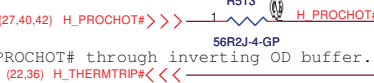
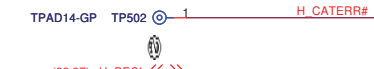
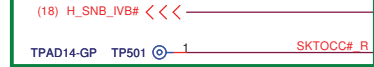
Stuff to disable internal graphics  
function for power saving.



SSID = CPU

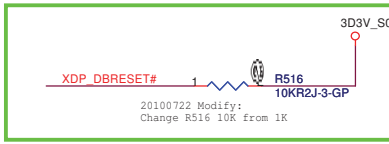
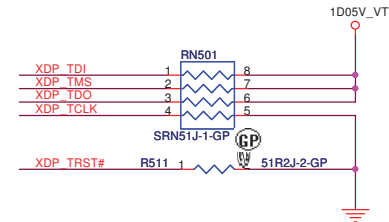
EDS R1.5:  
BGA have different name with rPGA

X00 1008



Disabling Guidelines:  
If motherboard only supports external graphics:  
Connect DPLL\_REF\_SSCLK on Processor to GND through 1K +/- 5% resistor.  
Connect DPLL\_REF\_SSCLK# on Processor to VCCP through 1K +/- 5% resistor power (~15 mW) may be wasted.

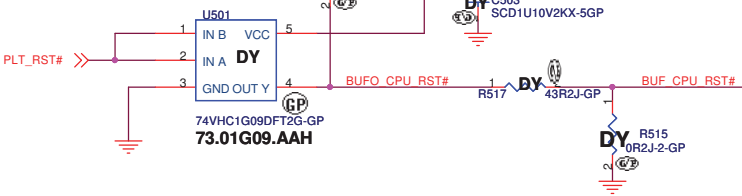
Signal Routing Guideline:  
SM\_RCOMP keep routing length less than 500 mils.



For XDP connector no enough space 6/28

0617 Modify: Joseph Removed U501 Buffer reset to CPU circuit.  
2010/07/19 Add buffer for PLT\_RST# based on Intel review.  
2010/07/20 DY buffer circuit and add R510, R509 and C501  
2010/07/20 Change U501 to 73.01G09.AAH

Buffered reset to CPU



<http://hobi-elektronika.net>

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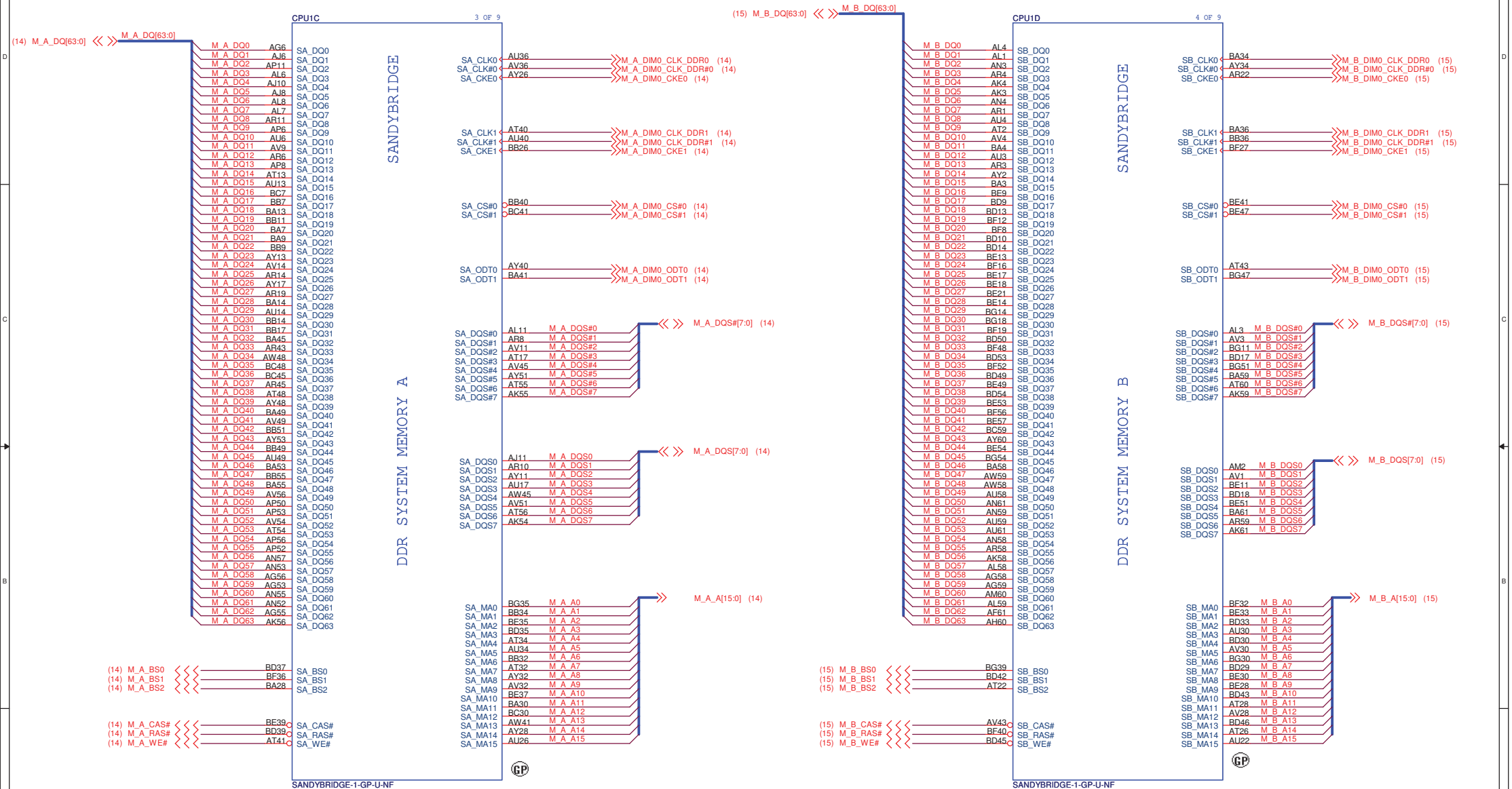
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Title: **CPU 2/7(THERMAL/CLOCK/PM)**

Size: Document Number: **DB13 DIS** Rev: **X00**

Date: Friday, November 26, 2010 Sheet: 5 of 105

SSID = CPU



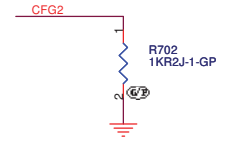
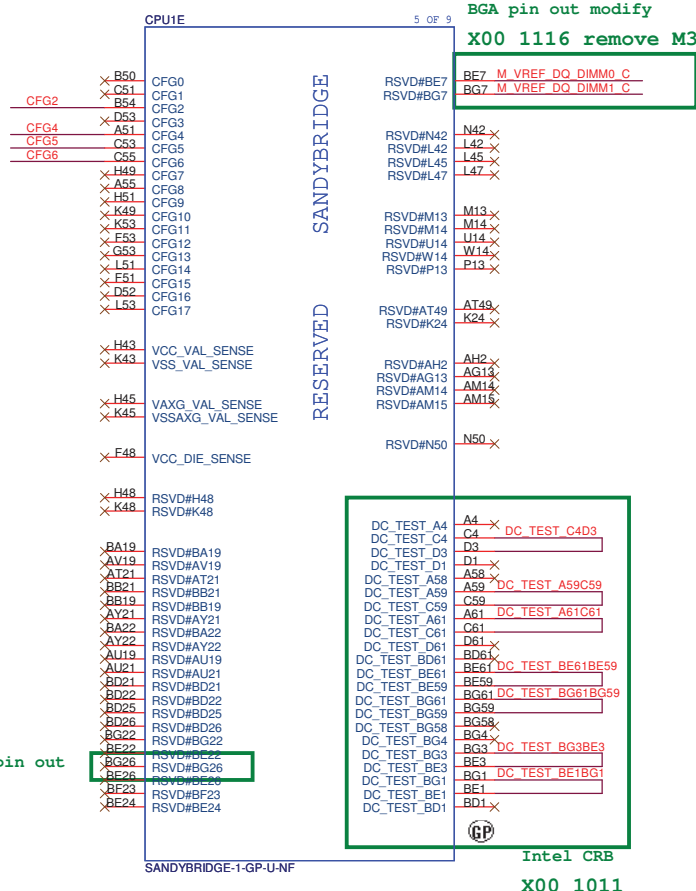
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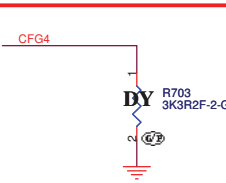
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Title			CPU 3/7(DDR)		
Size			Document Number		
Date:			Friday, November 26, 2010		
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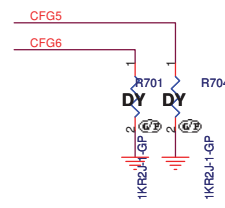
X00 1011



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

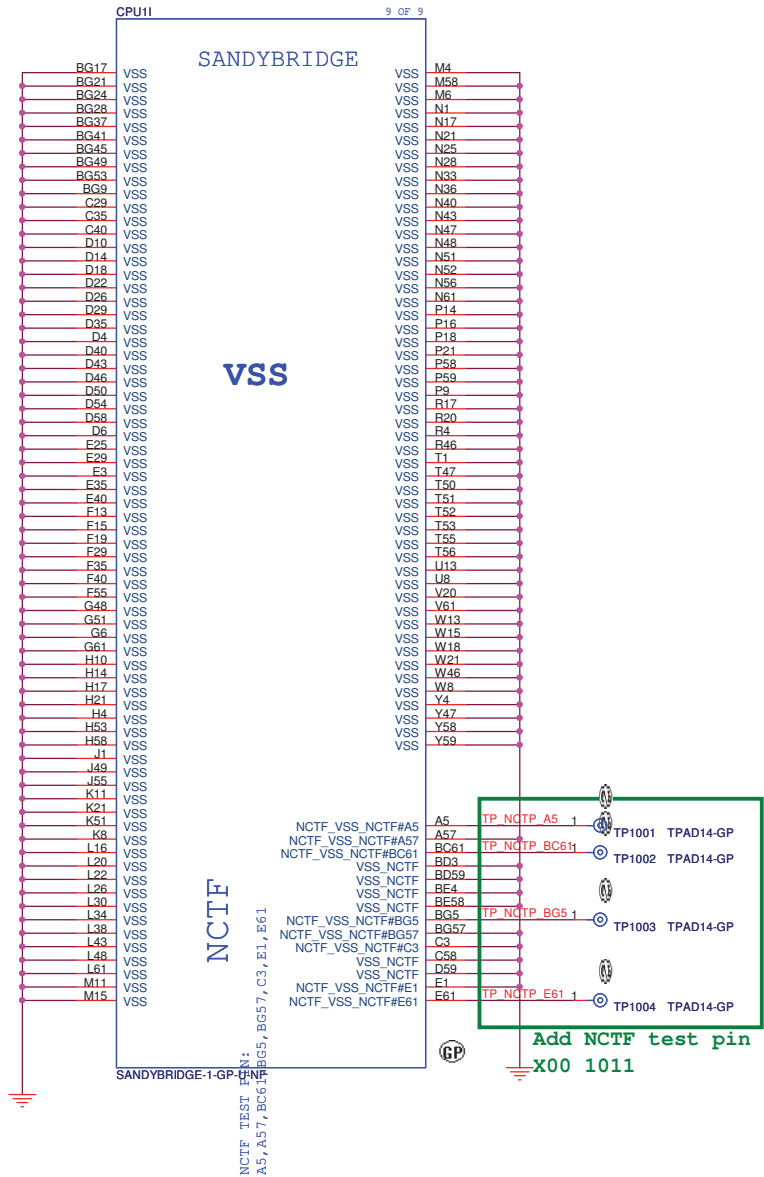
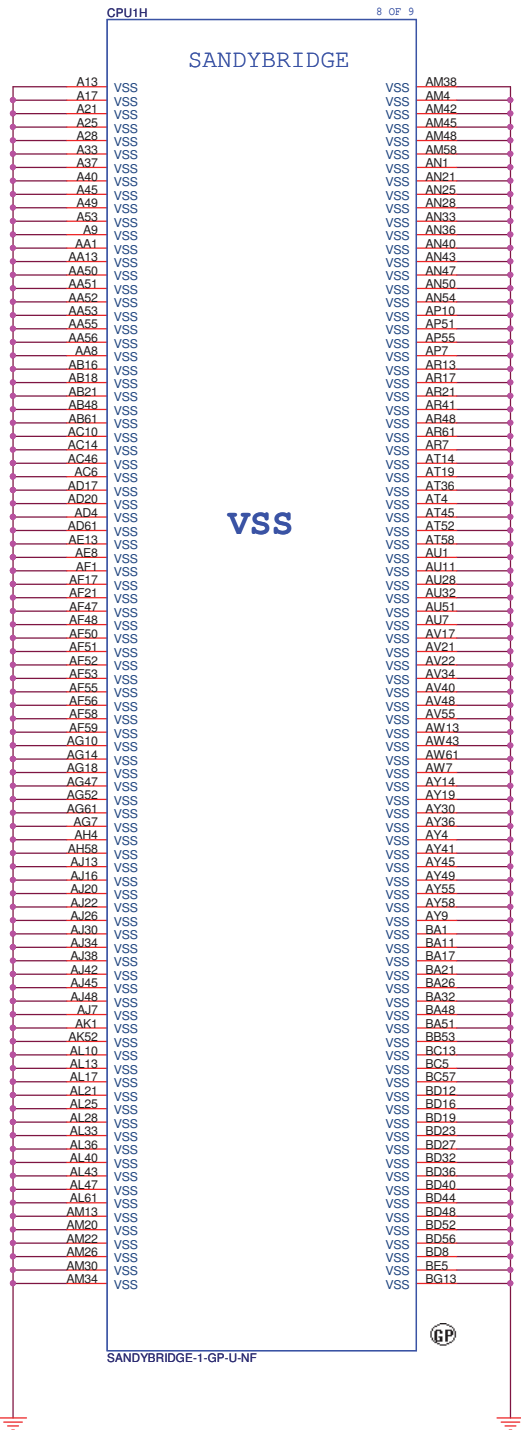
Remove to Page 8, BGA pin out  
X00 1011

X00 2010-11-16 Remove M3 - Processor Generated SO-DIMM VREF\_DQ





**SSID = CPU**



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Title

**CPU 7/7(VSS)**

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**DB13 DIS**


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Title

***Reserved***

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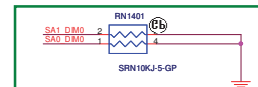
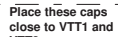
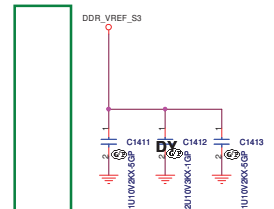
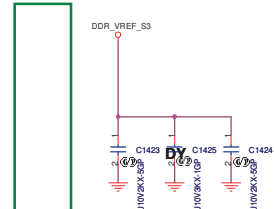


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Title

Reserved

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**Note:**  
If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30  
  
If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32



**Layout Note**  
Place these  
SO-DIMMs.


PART NUMBER	Height	TYPE
62.10017.W01	4.0mm	

H=4.0mm  
**62.10024.E21**



(Blanking)

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Title

*Reserved*

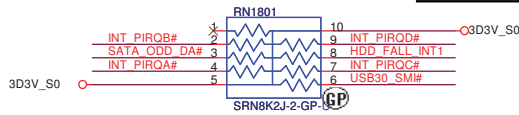
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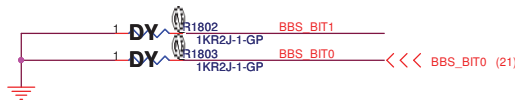
**SSID = PCH**

### USB 2.0 Overcurrent Pin Default Usage

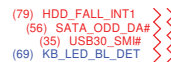
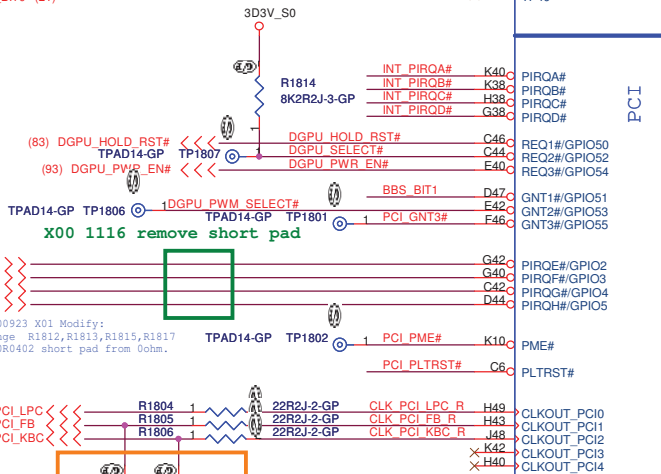
Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used



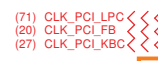
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)

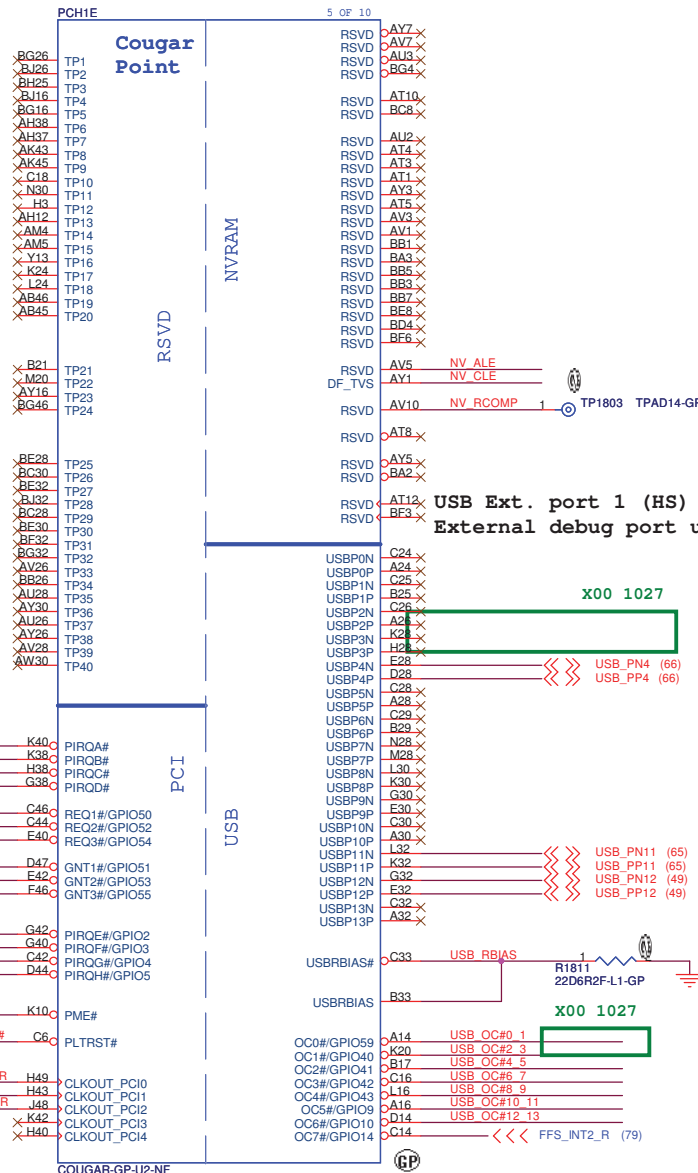
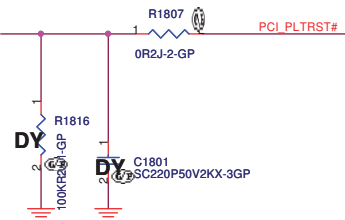


20100923 X01 Modify:  
Change R1812,R1813,R1815,R1817  
to 0R0402 short pad from 0ohm.



**KBC CLK EMI**

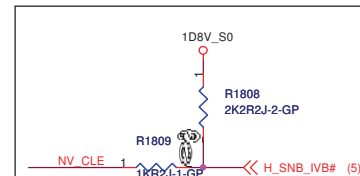
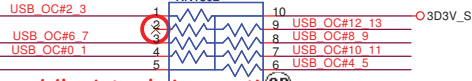
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20100908 X01 Modify:
Add R1818 10K PL on FFS_INT2_R(GPIO14)
```



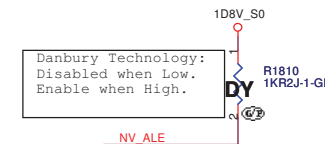
### USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

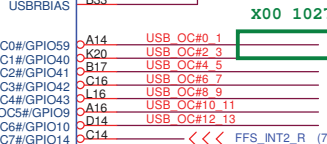
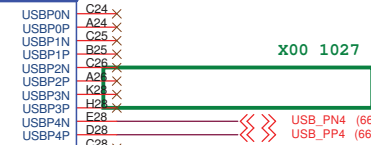
OC[3:0]# for Device 29 (Ports 0-7)  
OC[7:4]# for Device 26 (Ports 8-13)



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH



✗ USB Ext. port 1 (HS)  
✗ External debug port use on Huron river platform



## USB Table

Pair	Device
0	X
1	X
2	X
3	X
4	Mini Card2 (WWAN)
5	X
6	X
7	X
8	X
9	X
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

&lt;Core Design



Title	<b>PCH 2/9(PCI/USB/NVRAM)</b>
-------	-------------------------------

Size	Document Number	Rev
	<b>DB13 DIS</b>	<b>X00</b>

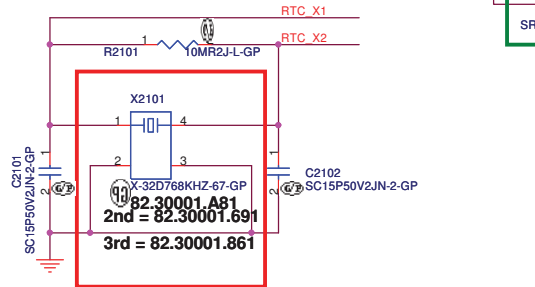
<http://hobi-elektronika.net>





# SSID = PCH

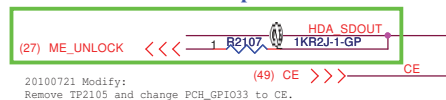
20100818 Sourcer suggest: Change X2101 as below.



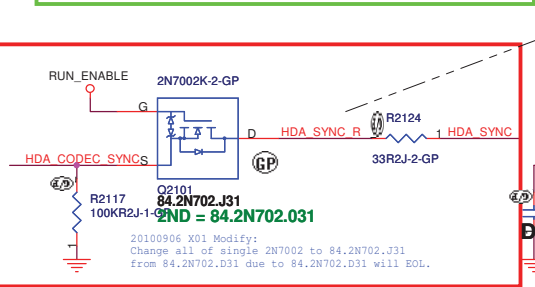
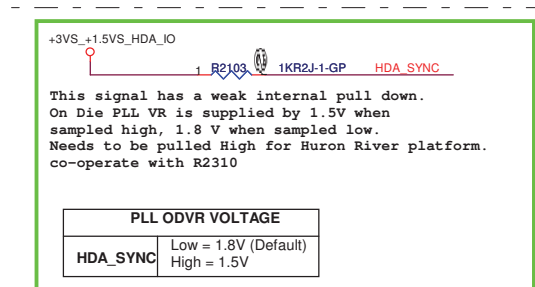
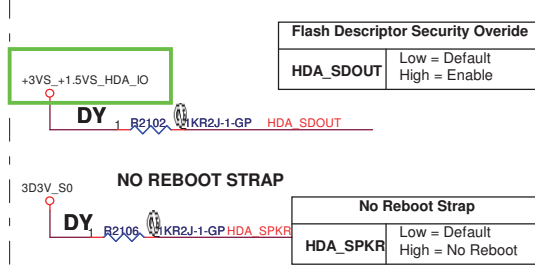
(29) HDA\_CODEC\_SYNC <<< 33R2J-2-GP  
(29) HDA\_CODEC\_SDOOUT <<< 33R2J-2-GP

(29) HDA\_CODEC\_RST# <<< 1  
(29) HDA\_CODEC\_BITCLK <<< 1

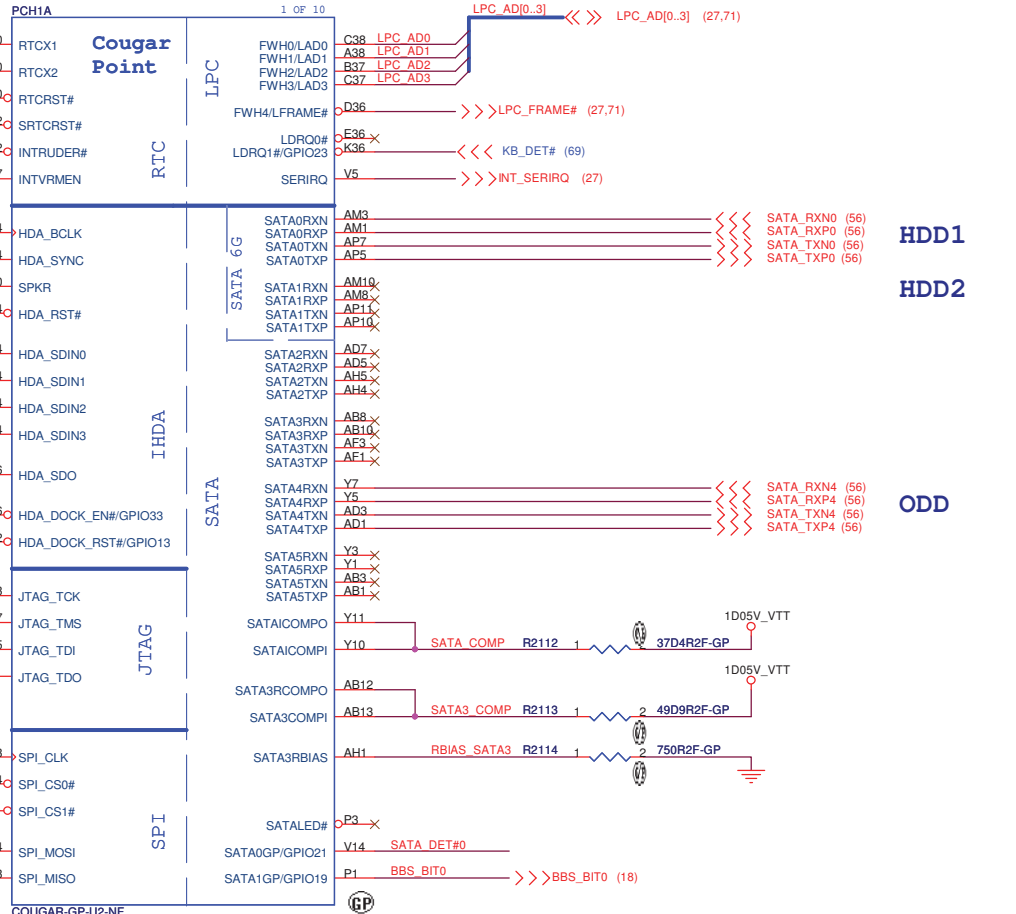
**Notes:**  
**ME\_UNLOCK (HDA\_SDO) connect to EC.**  
**Make sure EC drive this pin "low" all the time.**



20100721 Modify:  
Remove TP2105 and change PCH\_GPIO33 to CE.



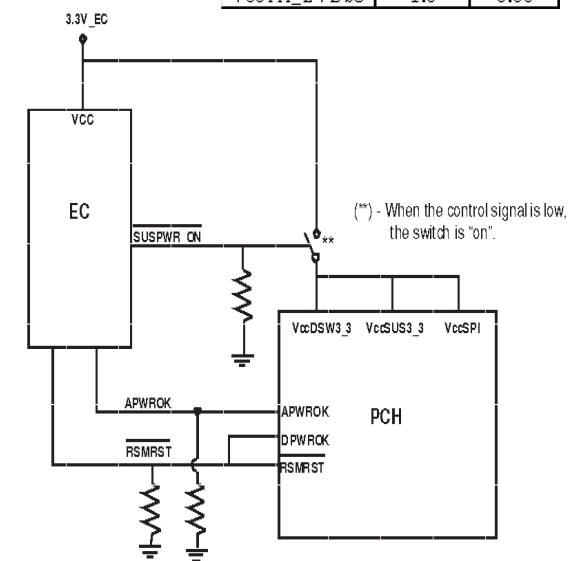
HDA\_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA\_SYNC from the Audio Codec device until after the Strap sampling is complete.



20100917 X01:  
Add RN2104 10K instead of R2111 10K.  
Move EC\_SC1#, DBC\_EN to RN2201. Remove RN2202.  
Change RN2103 to 10K array resistor to follow the standard schematics.  
Move S\_GPIO to RN2103. Move PSW\_CLR# to RN2104.  
20100921 X01:  
Swap SATA\_DET#0 and INT\_SERIRQ.



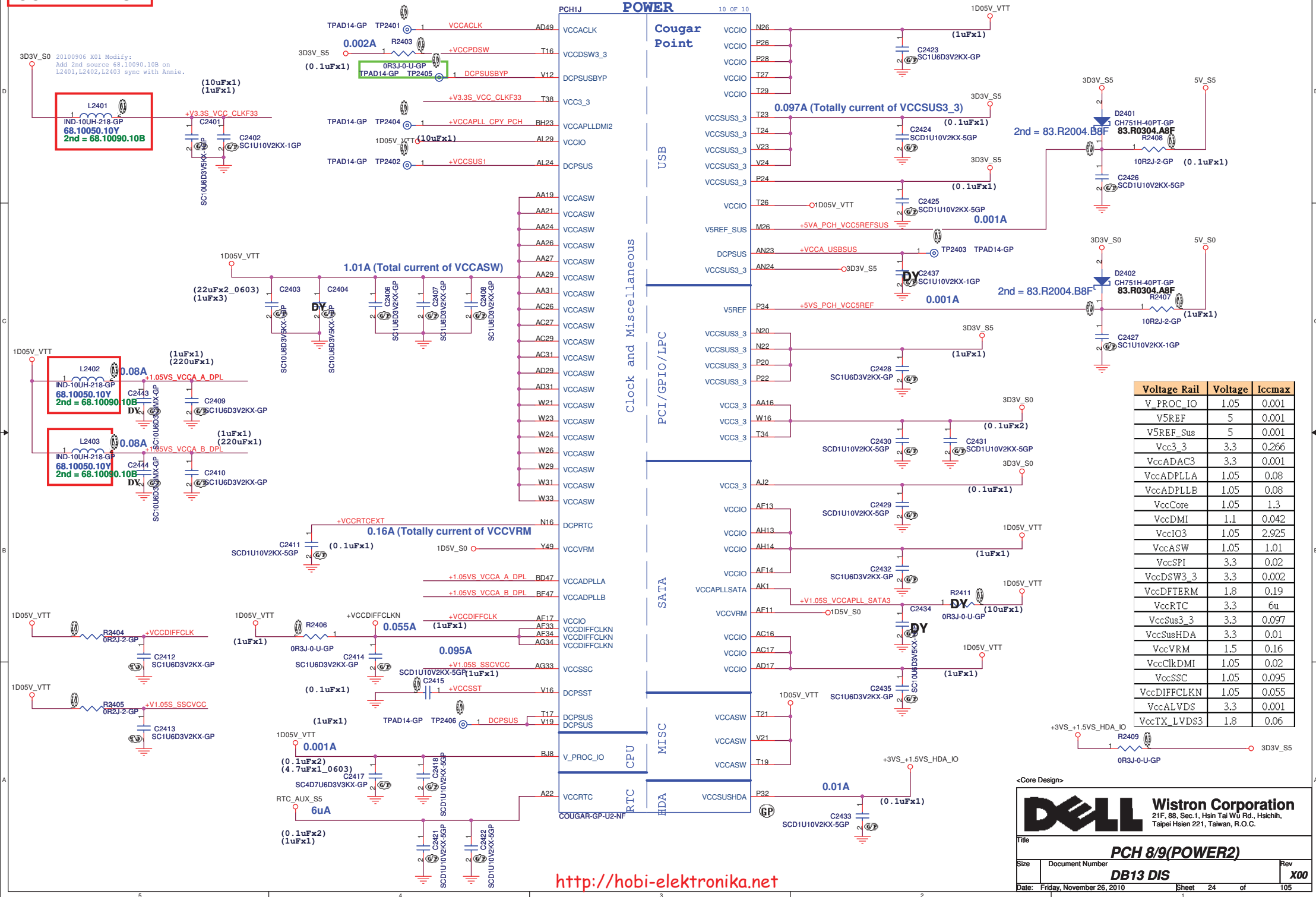
**6A**



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**SSID = PCH**



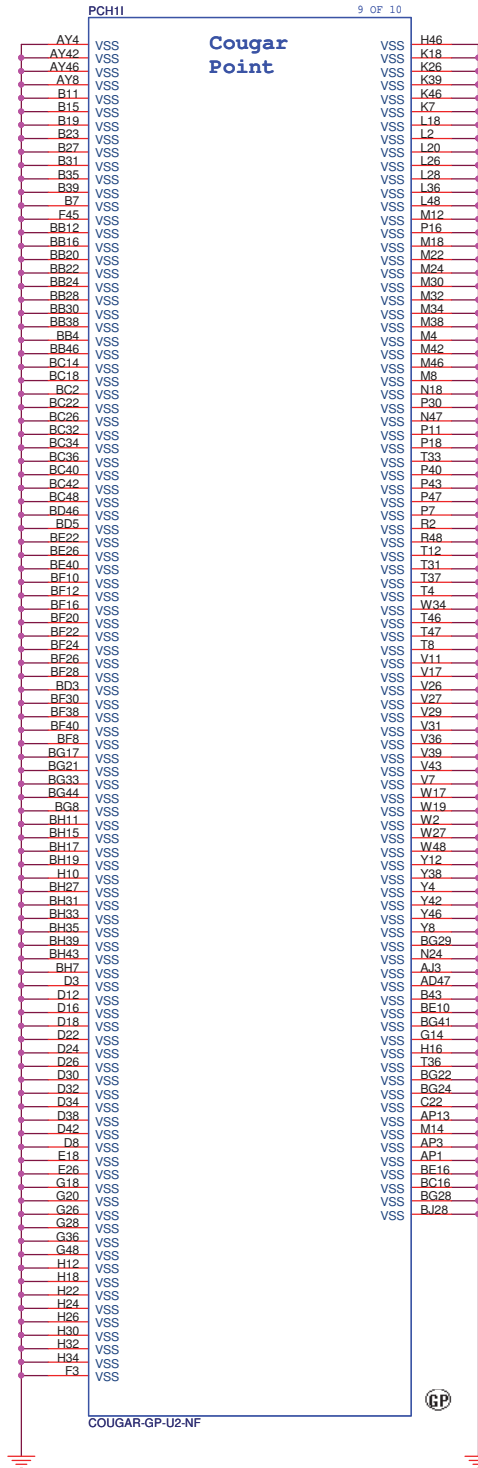
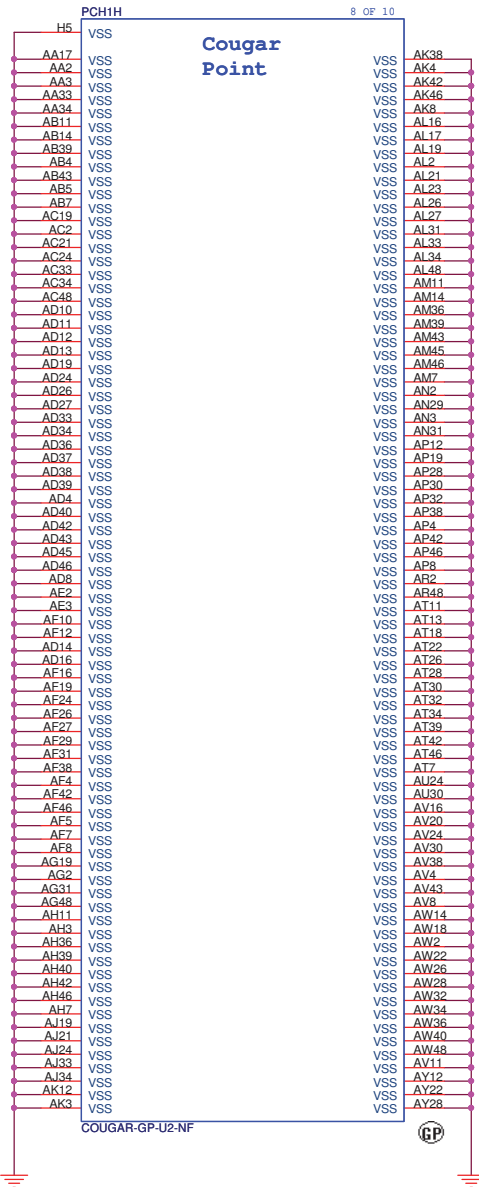
Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLL	1.05	0.08
VccADPLL	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTerm	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

### <Core Design>



Title			
<b>PCH 8/9(POWER2)</b>			
Size	Document Number	Rev	
	<b>DB13 DIS</b>	X	
Date:	Friday, November 26, 2010	Sheet	24 of 105

SSID = PCH



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<Core Design>




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Title			<b>PCH 9/9(VSS)</b>		
Size	Document Number				Rev
	<b>DB13 DIS</b>				<b>X00</b>
Date:	Friday, November 26, 2010		Sheet	25	of 105

(Blanking)

<Core Design>



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Title

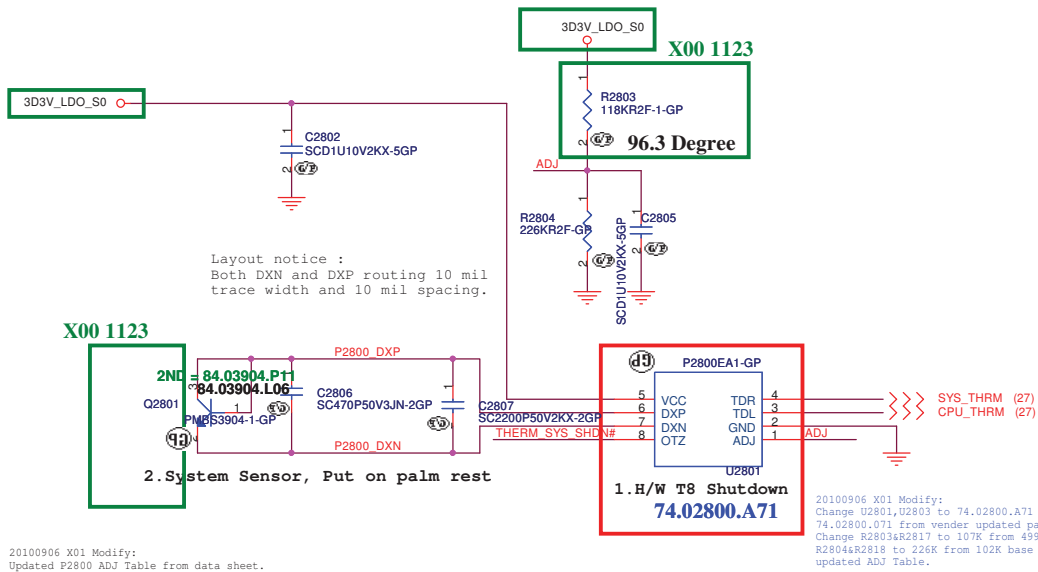
**Reserved**

Size	Document Number	Rev
A3	<b>DB13 DIS</b>	<b>X00</b>
Date:	Friday, November 26, 2010	Sheet 26 of 105



SSID = Thermal

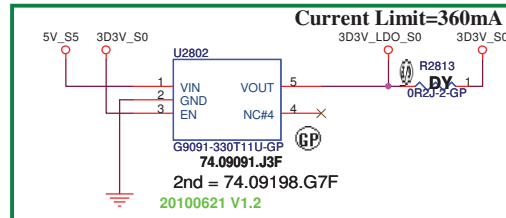
## Thermal sensor P2800



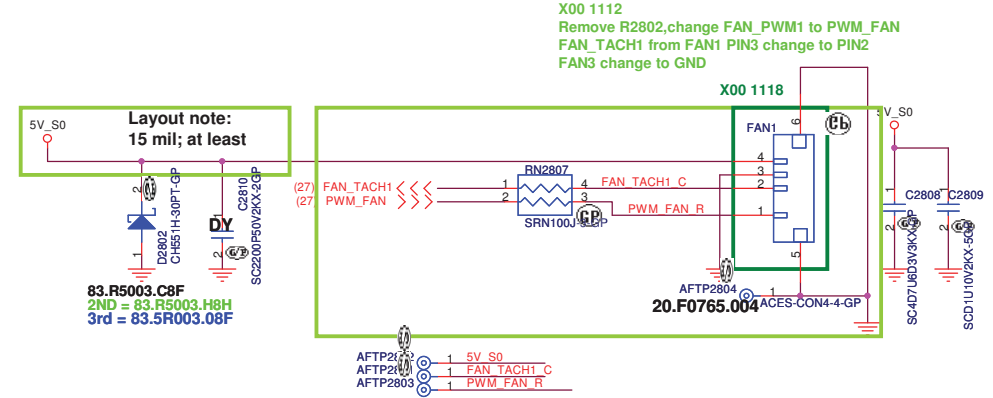
ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96  $\pm 1\%$  Series)

RADJ1 (K $\Omega$ )	RADJ2 (K $\Omega$ )	VADJ (V)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

X00 1123



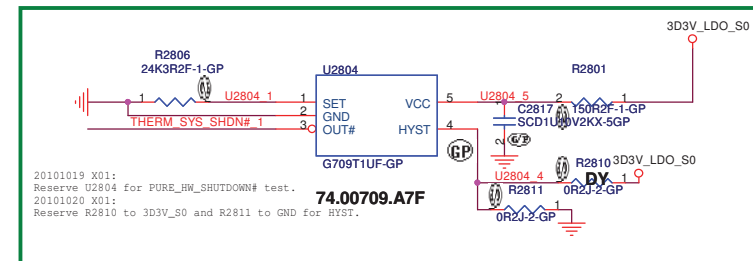
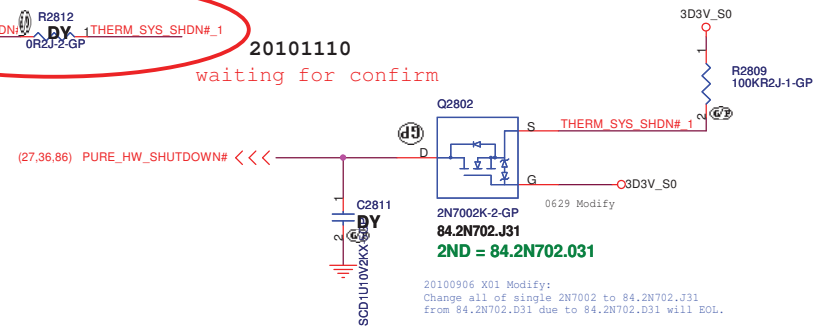
## PWM FAN CONN



THERM\_SYS\_SHDN# 1  
R2812  
0R2J-2-GP

20101110

waiting for confirm



X00 1123

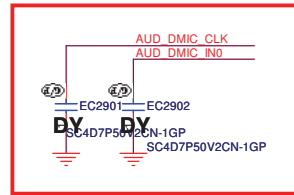
<Core Design>

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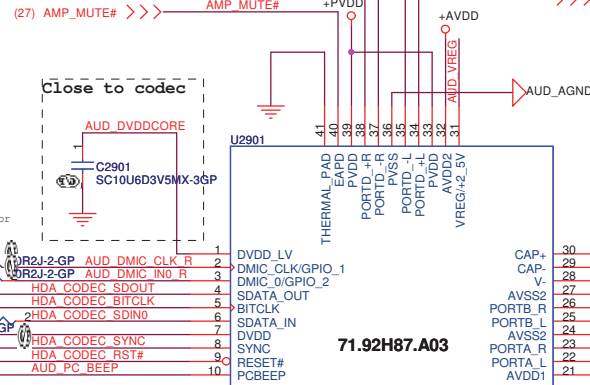
Title	THERMAL P2800 / Fan control		
Size	Document Number	Rev	X00
A3	DB13 DIS		
Date:	Friday, November 26, 2010	Sheet	28 of 105

# SSID = AUDIO

For EMI

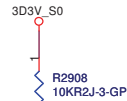
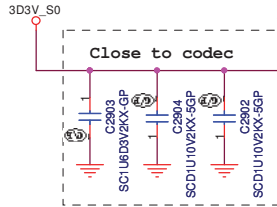


0625 Modify:  
AUD\_DMIC\_CLK&AUD\_DMIC\_IN0 connector  
to LVDS pin define.

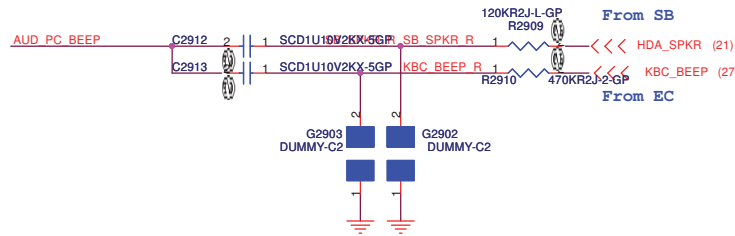


0707 Modify:  
updated U2901 part number from data base.

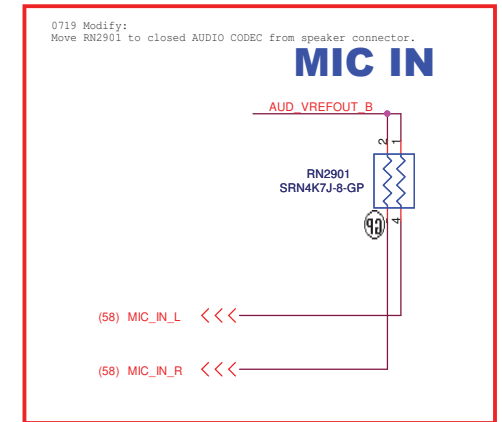
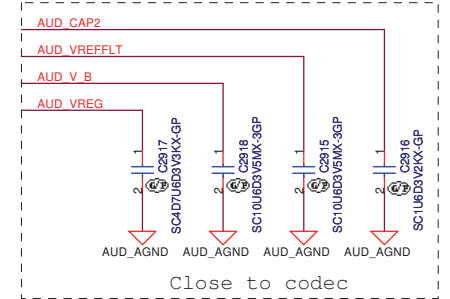
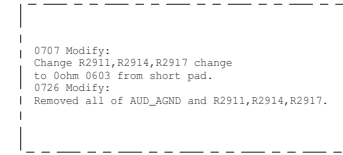
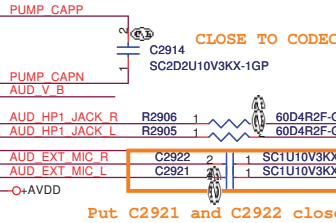
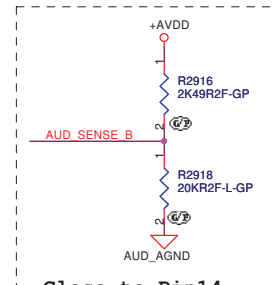
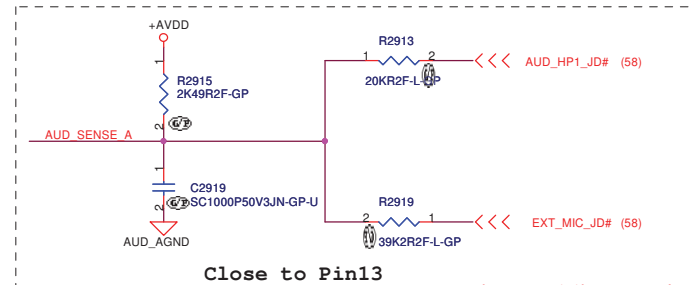
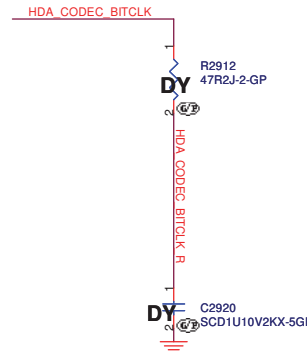
2010/06/30 Change to 92HD87 (71.92H87.A03)



AUD\_PC\_BEEP  
Trace width>15 mils




Azalia I/F EMI



<Core Design>

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<Core Design>



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Title

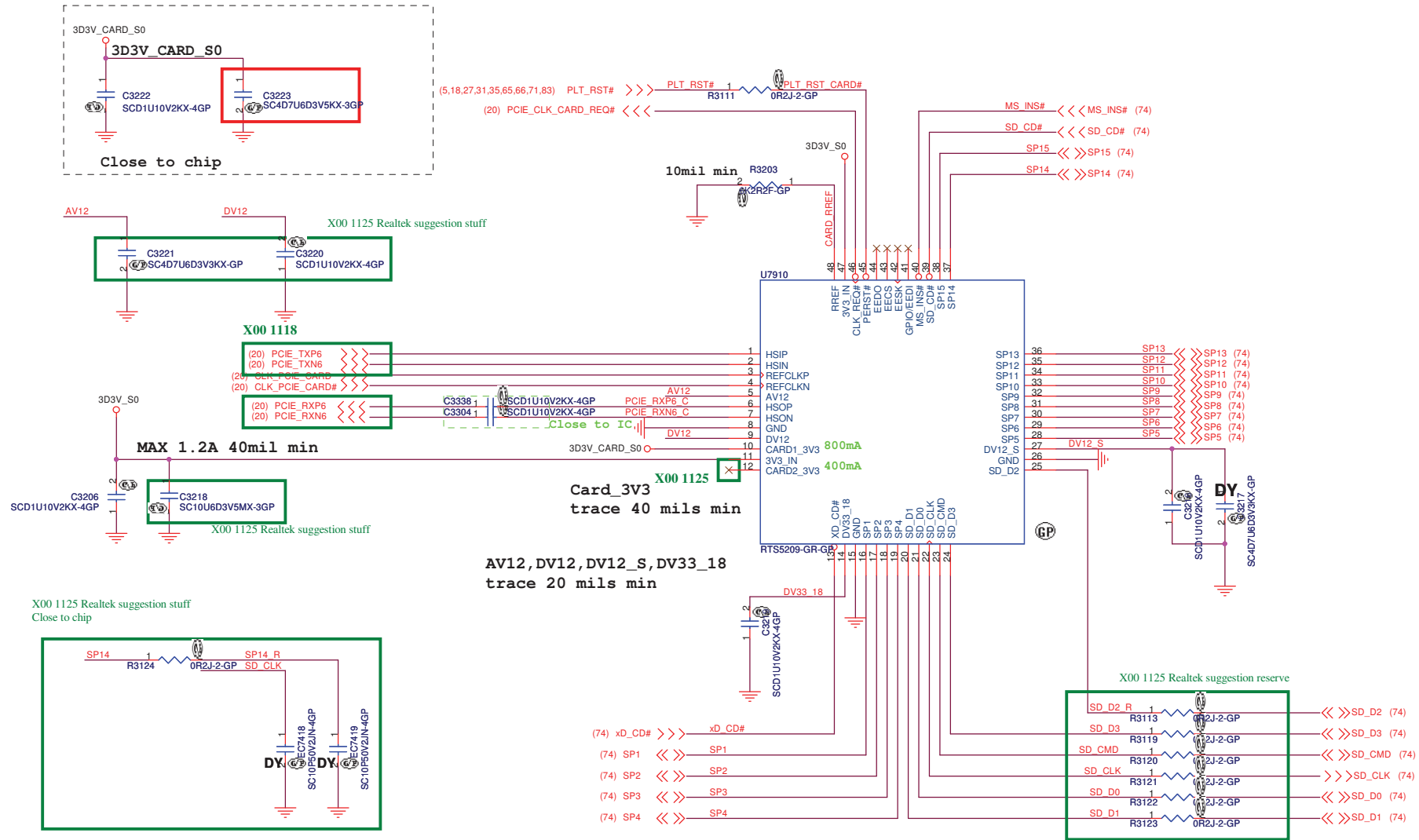
**Reserved**

Size	Document Number	Rev
A3	<b>DB13 DIS</b>	<b>X00</b>
Date:	Friday, November 26, 2010	Sheet 30 of 105

**SSID = LOM**



SSID = SDIO




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<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Card Reader RTS5209</b>			
Size A3	Document Number <b>DB13 DIS</b>	Rev <b>X00</b>	
Date: Friday, November 26, 2010	Sheet 32	of 105	



<Core Design>



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Title

**Reserved**

Size	Document Number	Rev
A3	<b>DB13 DIS</b>	<b>X00</b>
Date:	Friday, November 26, 2010	Sheet 33 of 105

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<Core Design>



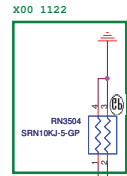
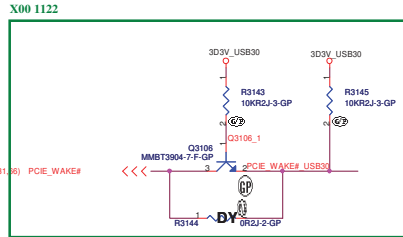
**Wistron Corporation**  
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Title

**Reserved**

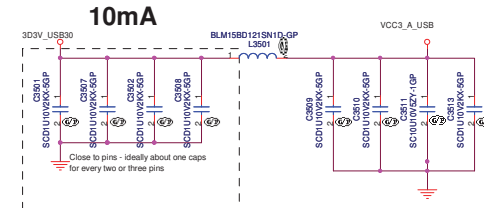
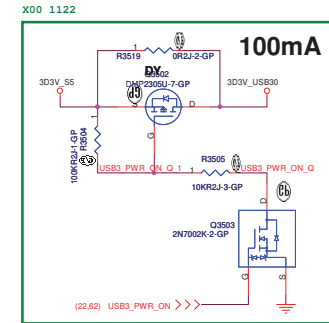
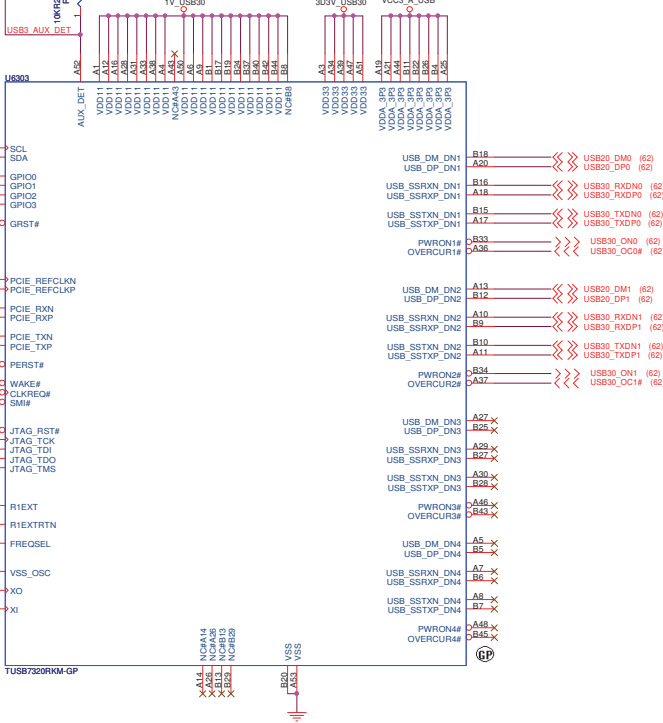
Size	Document Number	Rev
A3	<b>DB13 DIS</b>	<b>X00</b>
Date:	Friday, November 26, 2010	Sheet 34 of 105

Del two 50-ohm,when used PG1.5 sample.

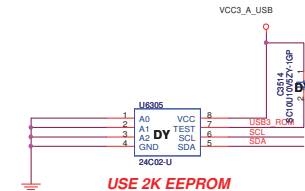
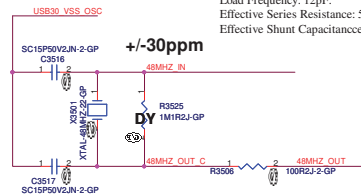


IF want to support S3 R6619 will pull high 3.3V

A43 & B8 IS NC PIN



HELE Recommended Conditions:  
Normal Frequency: 48MHz.  
Frequency Tolerance: +/- 30ppm.  
Load Frequency: 12pF.  
Effective Series Resistance: 50-ohm.  
Effective Shunt Capacitance: 2pF.

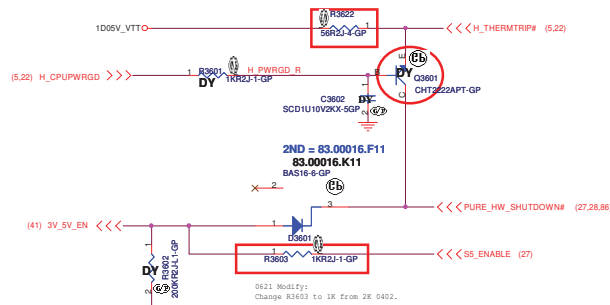


SSID = Reset.Suspend

(19,27) S0\_PWR\_GOOD >>> >>> SYS\_PWROK (19)

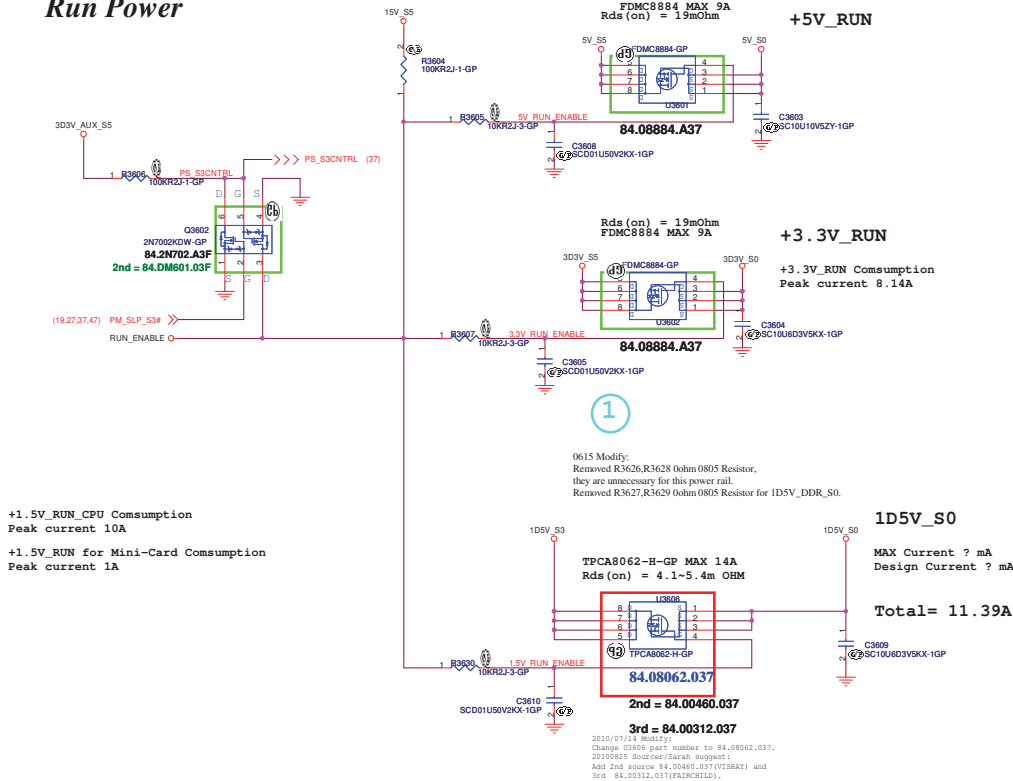
## Power Sequence

0628 Modify:  
Utilize D3602 Diode Instead of U3603 AND GATE  
for SYS\_PWROK sequence control.



SSID = Reset.Suspend

## Run Power

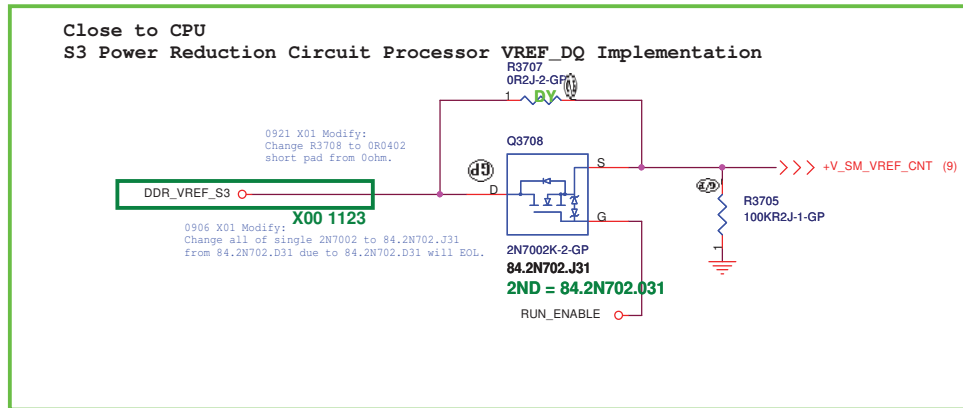


+1.5V\_RUN\_CPU Consumption  
Peak current 10A

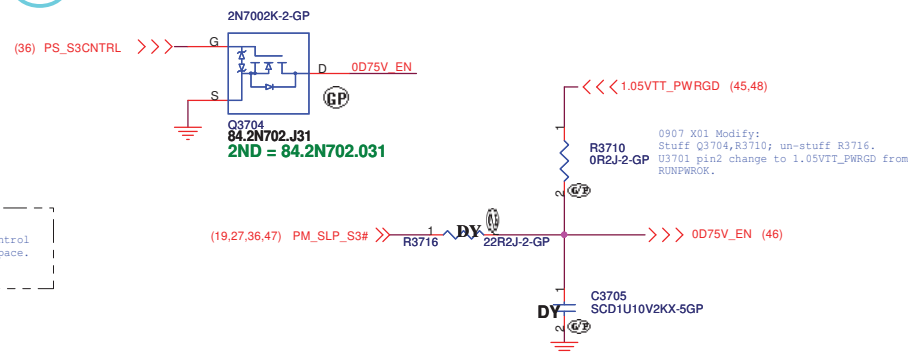
+1.5V\_RUN for Mini-Card Consumption  
Peak current 1A

<Core Design>

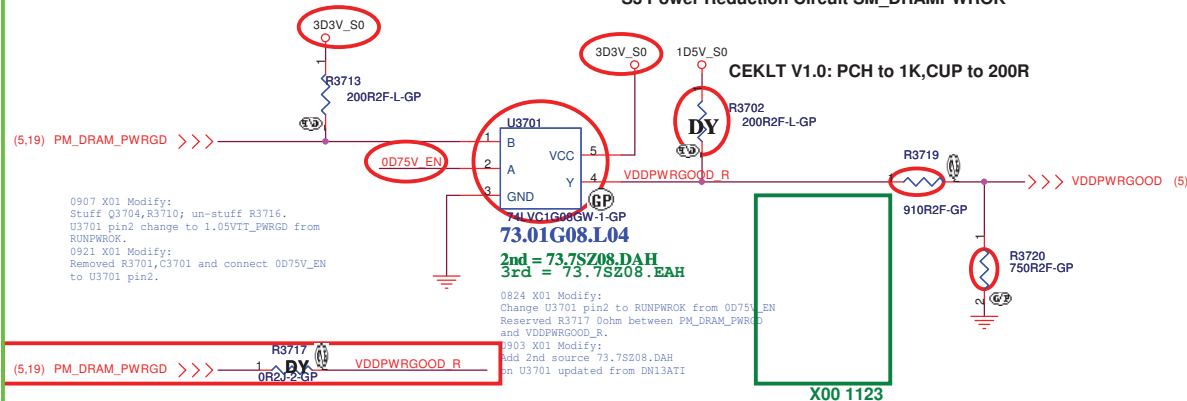
<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File			
<b>Power Plane Enable</b>			
Size A2	Document Number <b>DB13 DIS</b>	Rev <b>X00</b>	
Date: Friday, November 28, 2010		Sheet 36 of	106



**5 S3 Power Reduction X01 20091111**

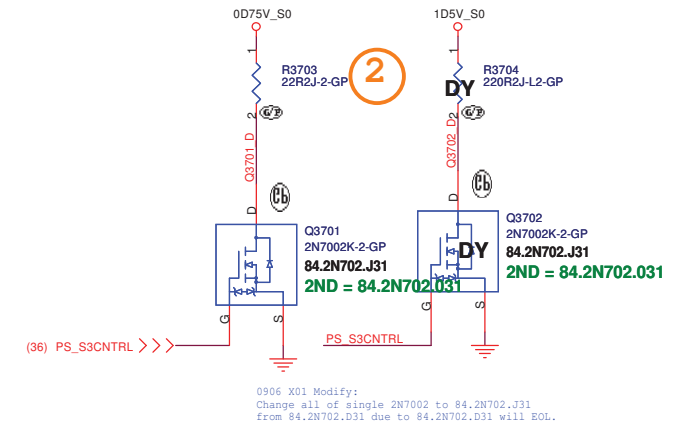


**Close to CPU**  
**S3 Power Reduction Circuit SM\_DRAMPWROK**

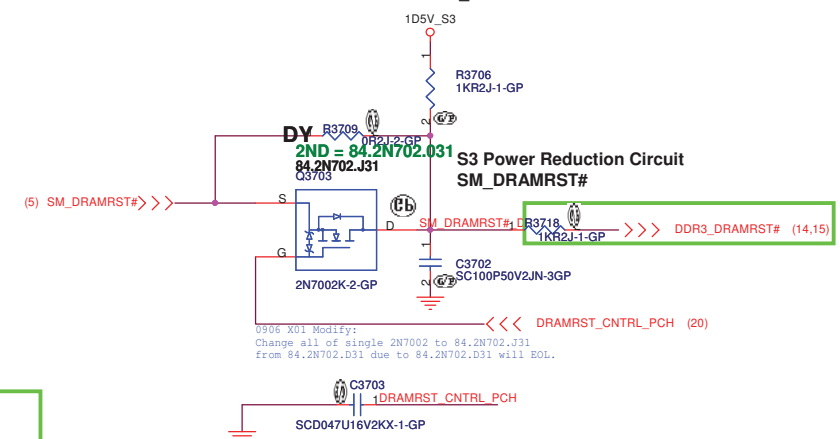


SM\_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ \* 0.55± 200mV and the edge must be monotonic

**Close to DIMM**  
**S3 Power Reduction Circuit SM\_DRAMPWROK**



**Close to CPU**  
**S3 Power Reduction Circuit SM\_DRAMPWROK**

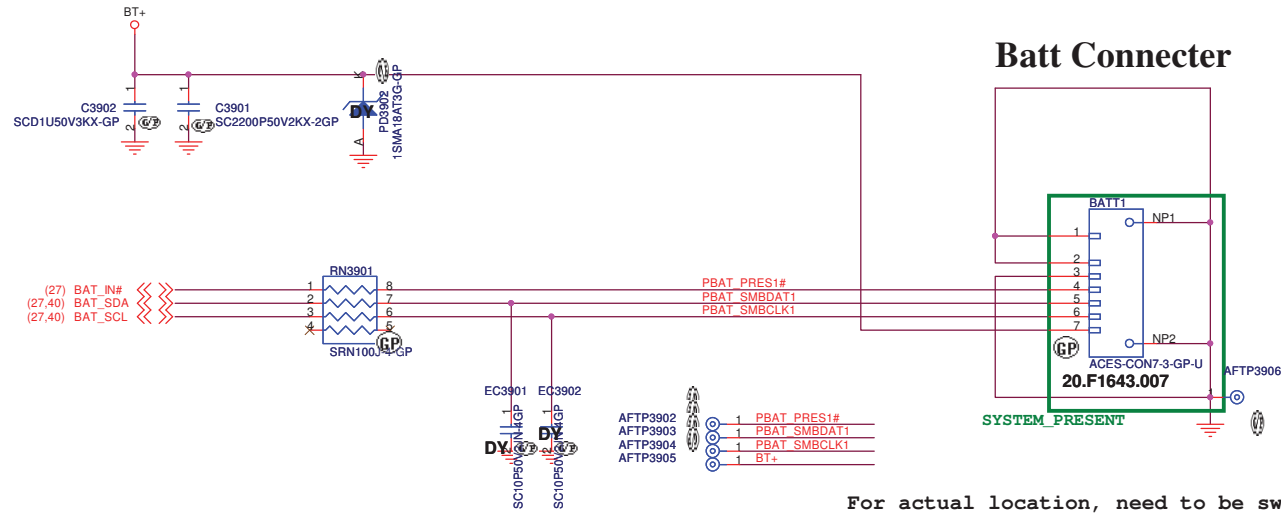


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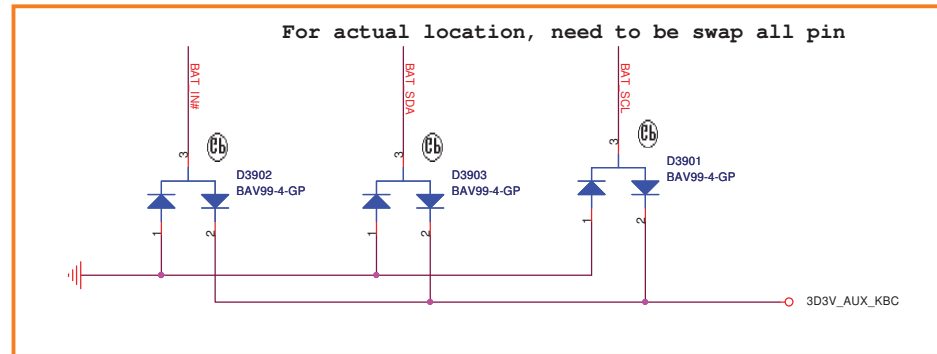
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b><i>S3 Power Reduction</i></b>			
Size A3	Document Number <b><i>XPS-Z 13</i></b>	Rev <b><i>X00</i></b>	
Date:	Friday, November 26, 2010	Sheet 37 of	105



SSID = BATT CONN



Close to Batt Connector

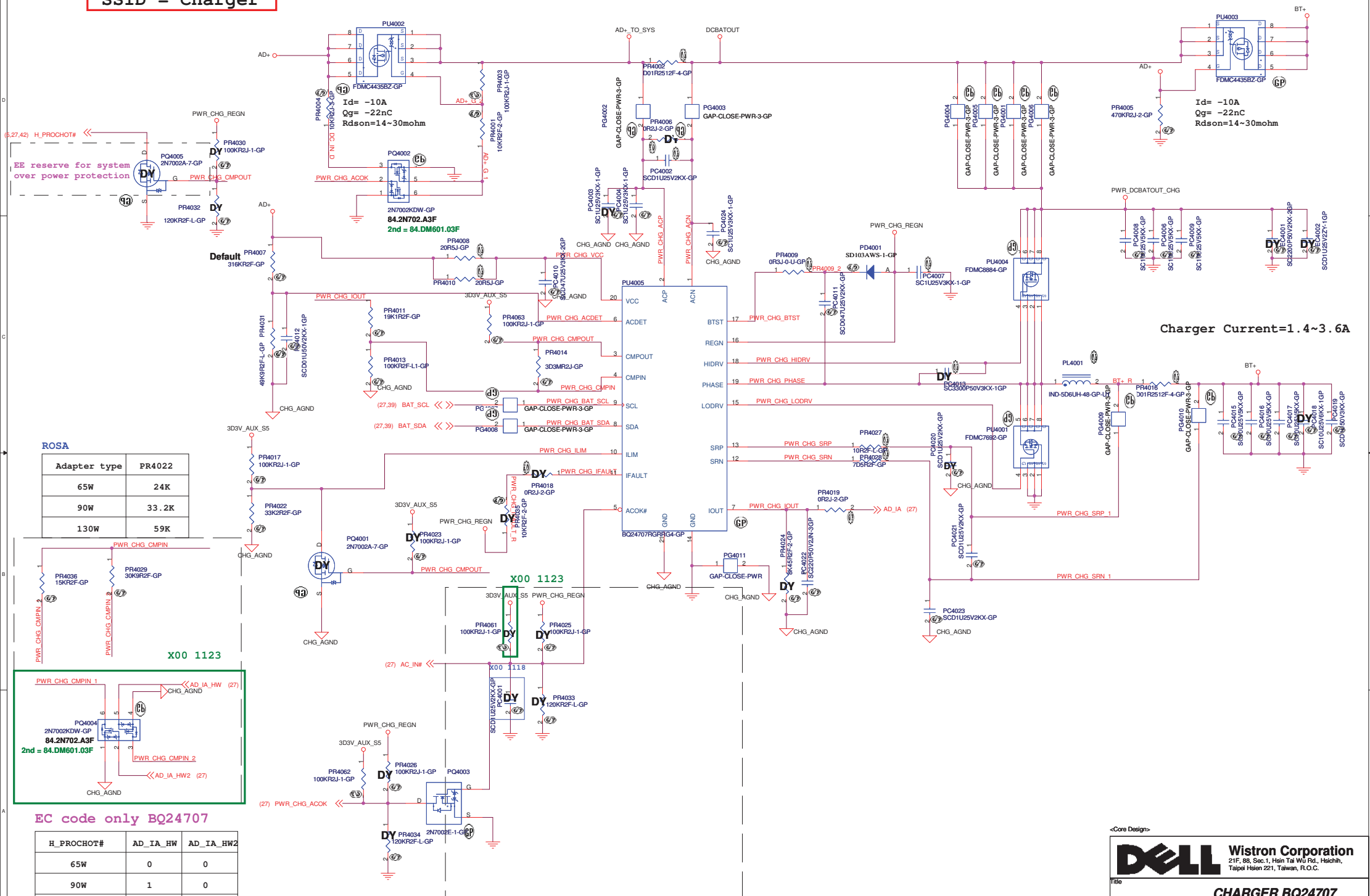


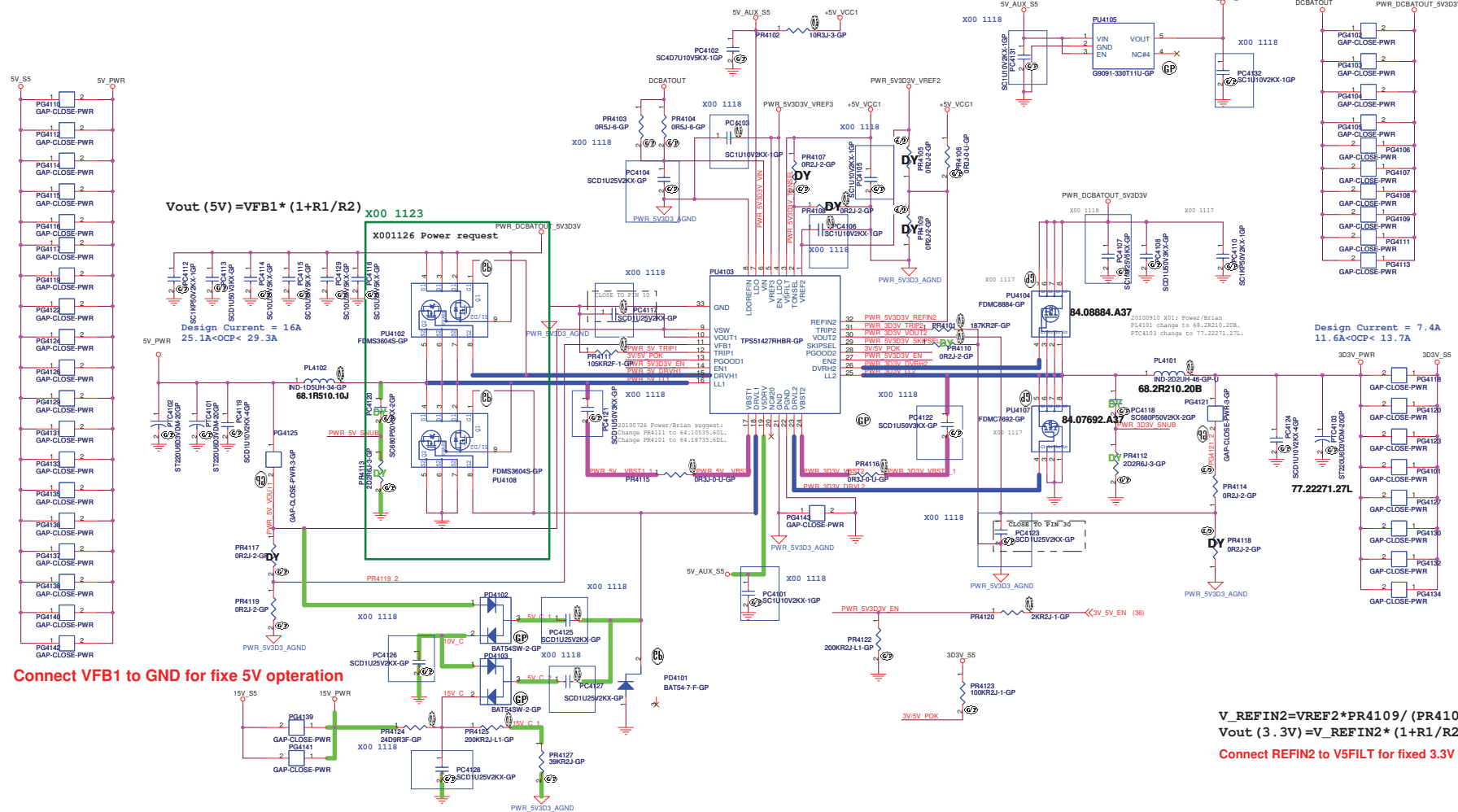
<http://hobi-elektronika.net>

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <b>BATT CONN</b>	
Size A3	Document Number <b>XPS-Z 13</b>	Rev <b>X00</b>	
Date: Friday, November 26, 2010	Sheet 39	of 105	

SSID = Charger



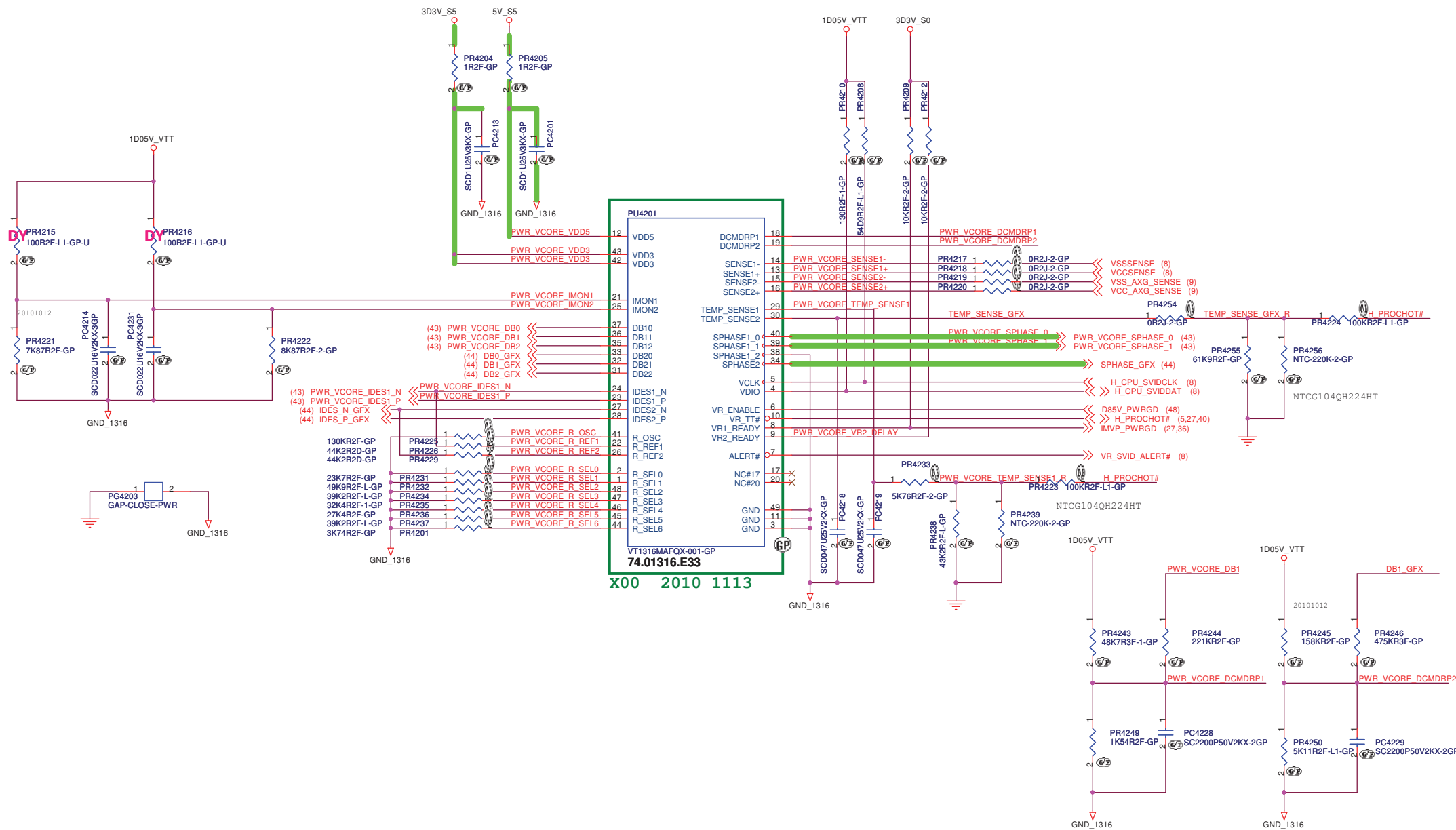


SKIPSEL Mode	GND Auto Skip	FLOAT/VREF2 OOA.	V5IN PWM Only
--------------	---------------	------------------	---------------

TONSEL	GND	VREF2 or Float	V5FILT
Ch1	400 kHz	400 kHz	200 kHz
Ch2	500 kHz	300 kHz	300 kHz

- 1A= 40mils
- 0.5A= 20mils
- 0.375A= 15mils

SSID = CPU.Regulator



<Core Design>

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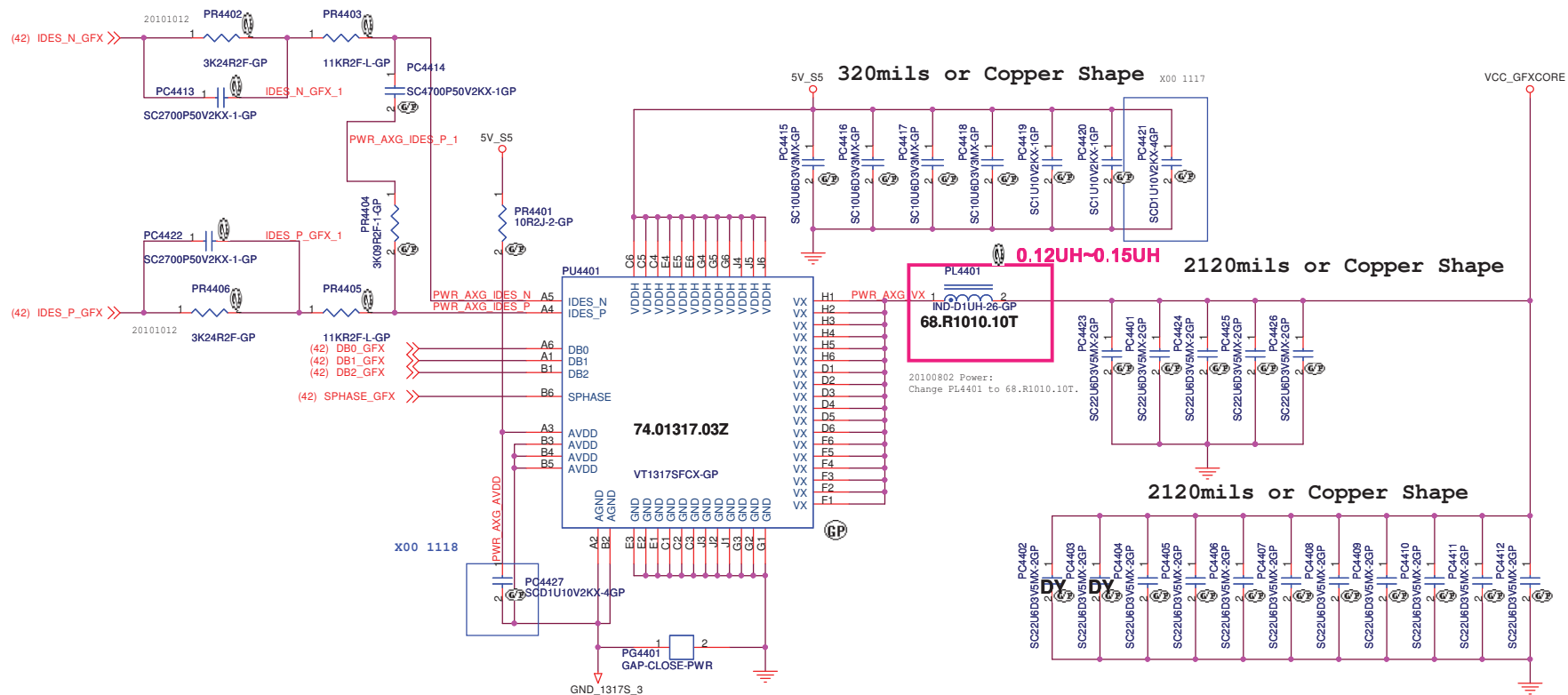
Title  
**VT1316+1314 CPU CORE(1/3)**

Size	Document Number	Rev
A3	<b>XPS-Z 13</b>	<b>X00</b>

Date: Friday, November 26, 2010 Sheet 42 of 105

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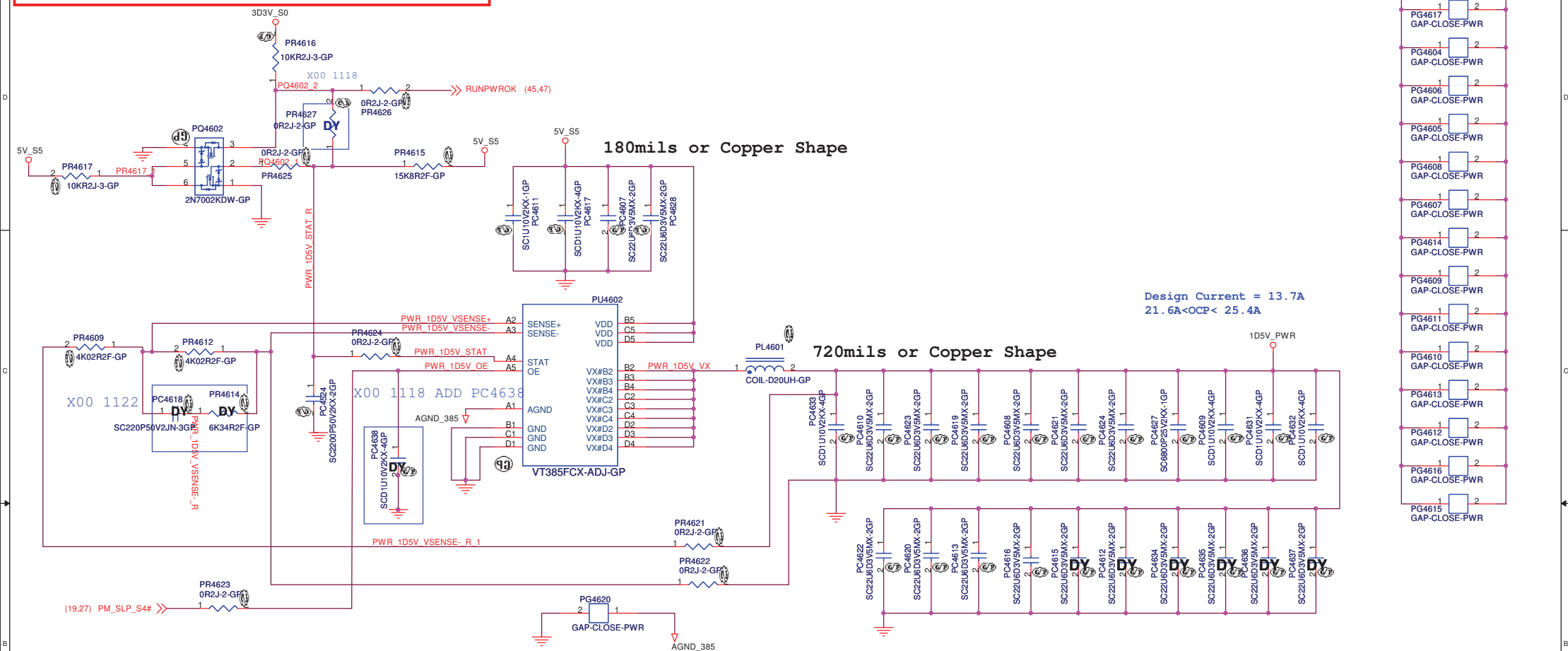
<Core Design>

**DELL** Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

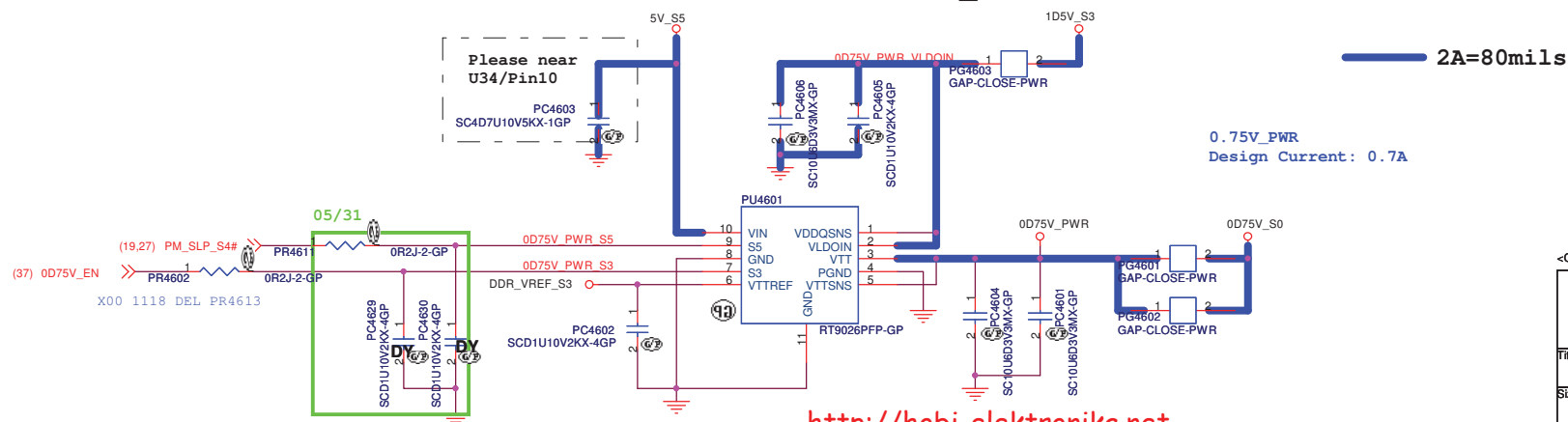
Title			VT1316+1317 AXG CORE(3/3)	
Size	Document Number	Rev		
A3	XPS-Z 13	X00		
Date:	Friday, November 26, 2010	Sheet	44	of 105



```
SSID = PWR.Plane.Regulator_1p5v0p75v
```



## RT9026 for 0D75V\_S0



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## <Core Design>

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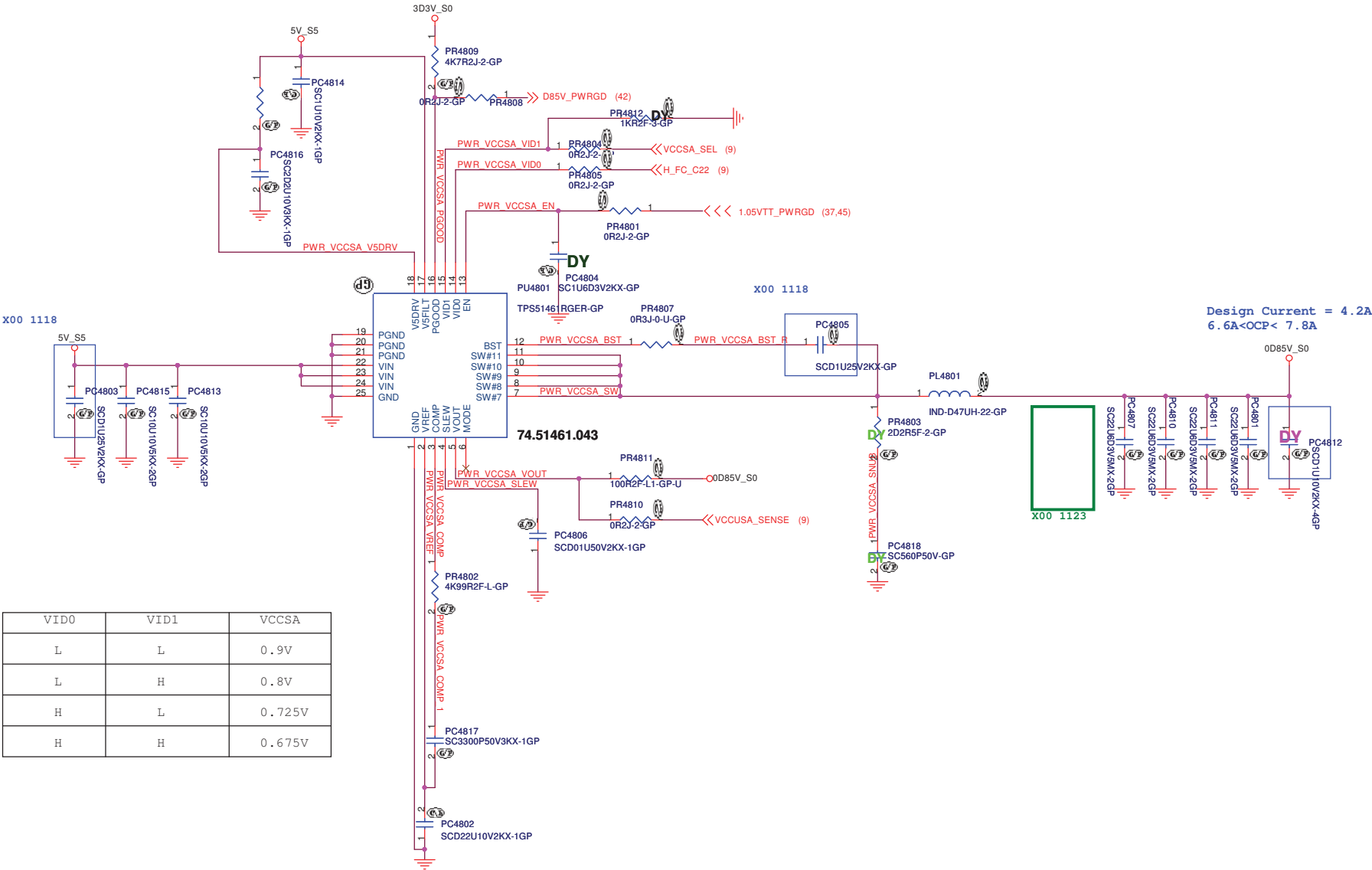
Title	<b>VT385 +1.5V SUS/+0.75V SUS</b>
-------	-----------------------------------

Size A3	Document Number <b>XPS-Z 13</b>	Rev <b>X00</b>
------------	------------------------------------	-------------------

Date: Friday, November 26, 2010	Sheet 46 of 105
---------------------------------	-----------------



TPS51461 for VCCSA

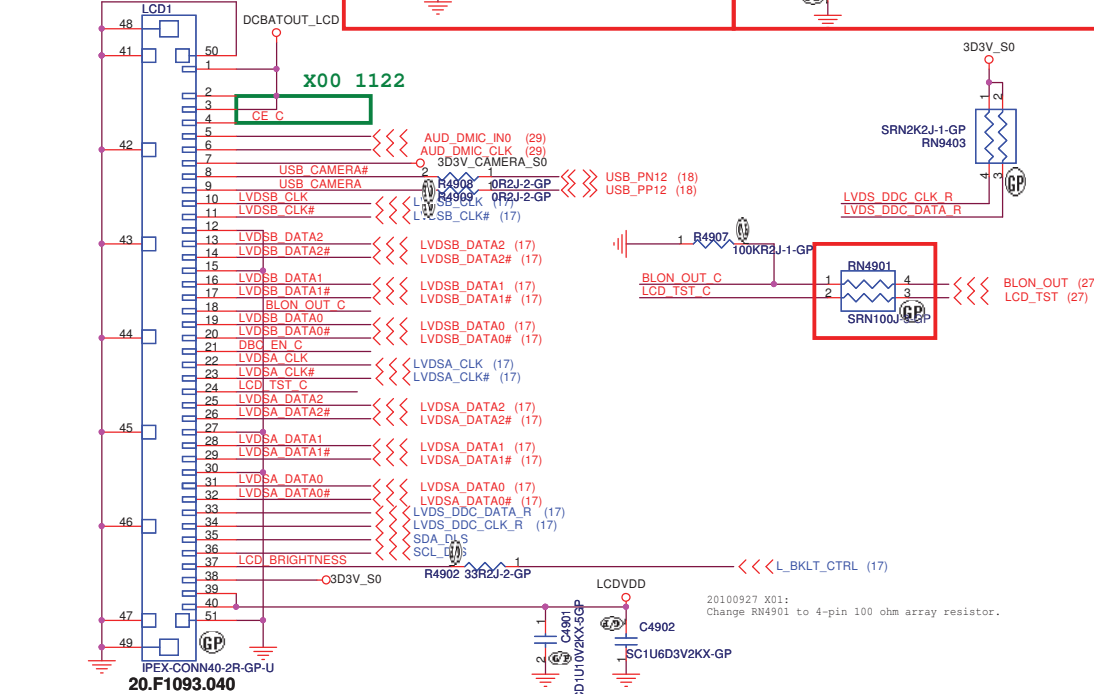


SSID = VIDEO

20100927 X01:  
Change LCD1 to 20.F1816.030 (30 pins),  
reassign pin definition and remove CE\_C.  
Add PD4901 to protect EC.

20100721 Modify:  
Add CE\_C control circuit and connect to PCH GPI033.  
20100927 X01:  
Connect CE\_C to LCD1.15.

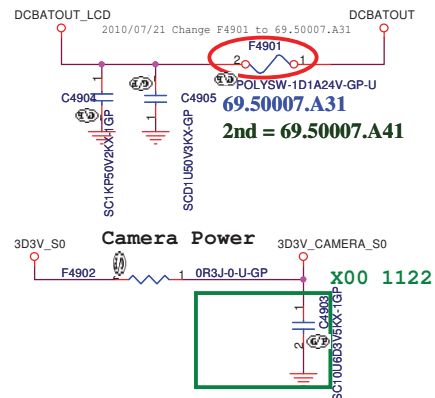
## LVDS CONNECTOR



## CAMERA and DIGITAL MIC PIN DEFINE!

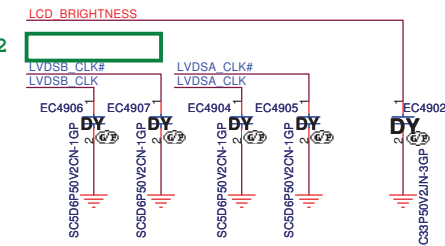
Pin No.	Name	Pin Type	Function Description
1	Flag_Loop	PNP	Cable Connection Identification
2	D+	Data Pin	USB Data Transmission
3	D-	Data Pin	USB Data Transmission
4	USB+3V	Power Pin	Power Supply
5	DMIC_L_VIN	Data Pin	Digital MIC CLK#
6	DMIC_GND	GND	Digital MIC GND
7	DMIC_DIN0A	Data Pin	Digital MIC DATA
8	GND	GND	System Ground

20100920 X01 EMI/Simon request:  
LVDSA\_DATA0#, LVDSA\_DATA0#, LVDSA\_DATA1#, LVDSA\_DATA1#, LVDSA\_DATA2#, LVDSA\_DATA2#  
add series 0 ohm resistor and grounding 10p capacitance.  
Add 0 ohm series 0 ohm resistors at LVDSA\_CLK# and LVDSA\_CLK.



X00 1122

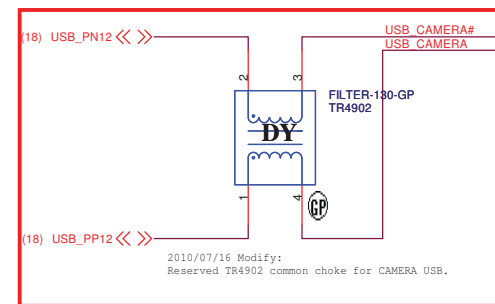
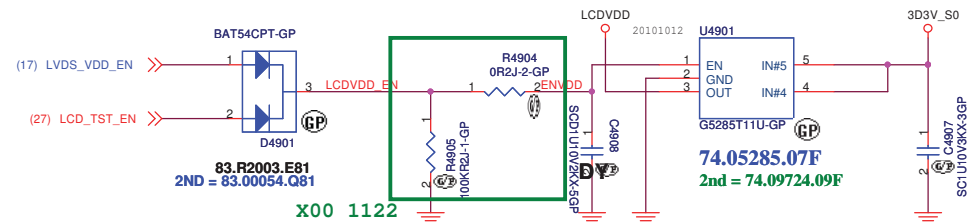
For EMI request  
Close to LVDS connector



SSID = VIDEO

## LCD POWER for ROSA

20100906 X01 Modify:  
Add 2nd source 74.09724.09F on  
U4901 sync with Annie.




2010/07/16 Modify:  
Reserved TR4902 common choke for CAMERA USB.

<Core Design>

<b>DELL</b>			<b>Wistron Corporation</b>		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.					
Title: <b>LCD/Inverter Connector</b>					
Size: A3	Document Number: <b>DB13 DIS</b>				Rev: <b>X00</b>
Date: Friday, November 26, 2010	Sheet: 49		of 105		

(Blanking)

<Core Design>



Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
A3

Document Number  
**DB13 DIS**

Date: Friday, November 26, 2010

Rev  
**X00**

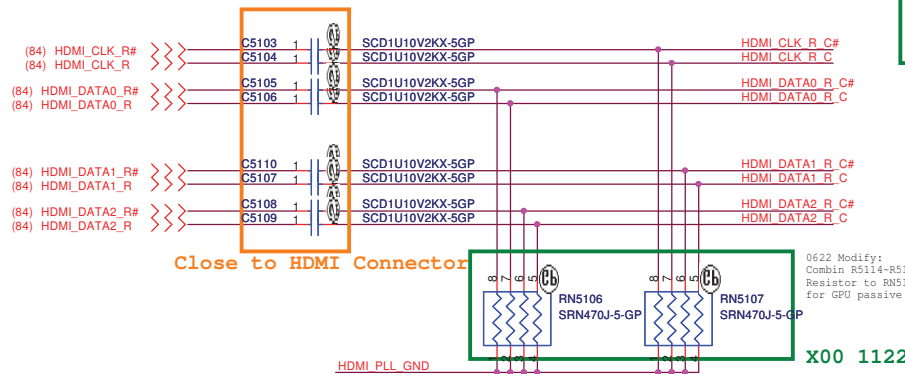
Sheet 50 of 105

SSID = VIDEO

# HDMI Level Shifter & CONNECTOR

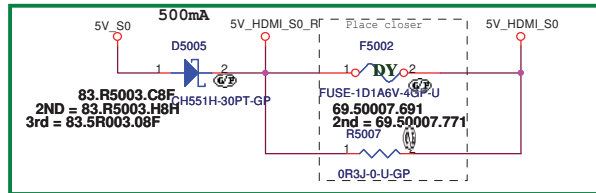
Removed LEVEL SHIFTER base on DELL feedback spec.  
(No support 220MHZ deep color mode, so can be removed  
HDMI LEVEL SHIFTER circuit.

2010/07/21 Delete RN5112, RN5113, RN5114, and RN5115 and short these traces.  
20100902 Add OR(R5101-R5108) for HDMI tuning.



suggestion to stuff 470-ohm for NV.

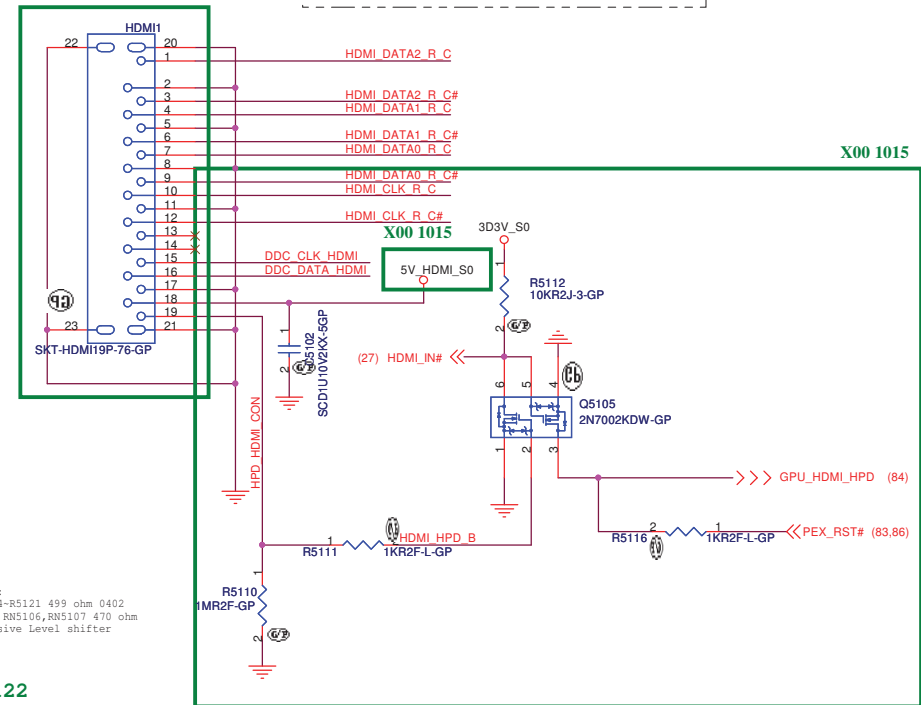
X00 1015



## HDMI CONN

X00 1108

Removed HDMI\_IN# CIRCUIT  
connect to KBC GPIO.



X00 1015

X00 1122

## Routing Guidelines:

CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).

The total delay on CTRLDATA should be longer than CTRLCLK.

<Core Design>


**DELL** Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			HDMI Level Shifter/Connector	
Size	Document Number	DB13 DIS		Rev
A3				X00
Date:	Friday, November 26, 2010	Sheet	51	of 105



(Blanking)

<Core Design>



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Title

**LVDS Switch**

Size	Document Number	Rev
A3	<b>DB13 DIS</b>	<b>X00</b>
Date:	Friday, November 26, 2010	Sheet 53 of 105

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size  
A3

Document Number  
DB13 DIS

Date: Friday, November 26, 2010

Sheet  
54

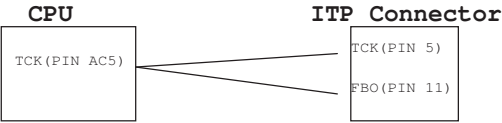
of  
105

Rev  
X00

SSID = User.Interface

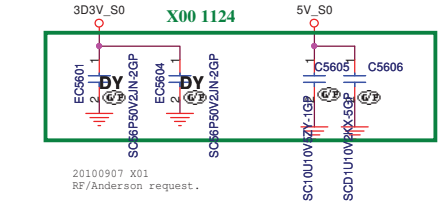
ITP Connector

H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.

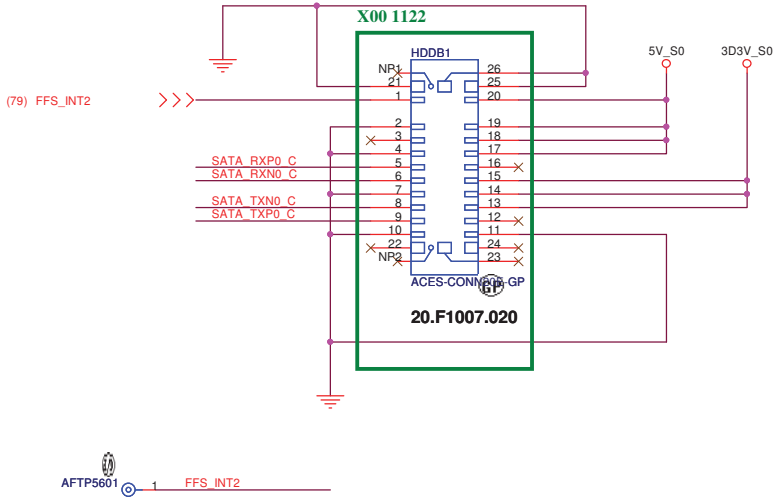
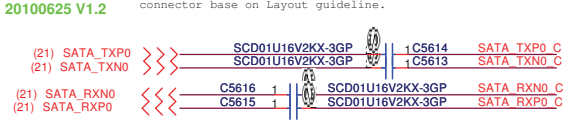


SSID = SATA

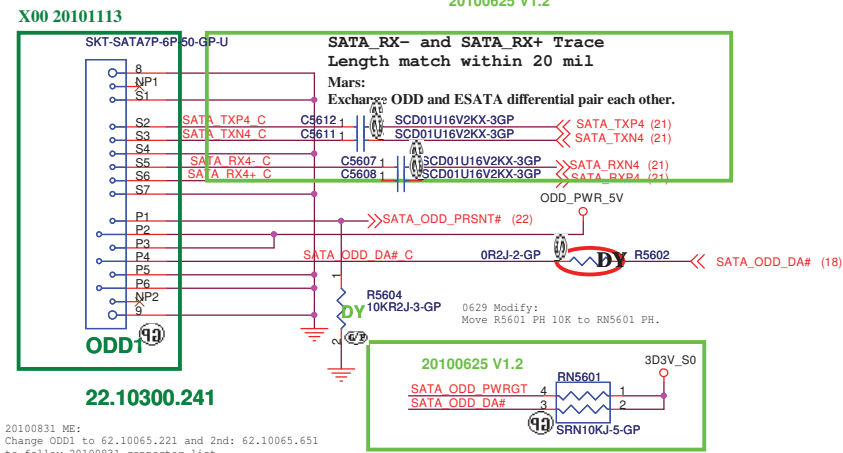
# SATA HDD Connector



0629 Modify:  
Move All of 0.01uF cap closed to HDD connector base on Layout guideline.

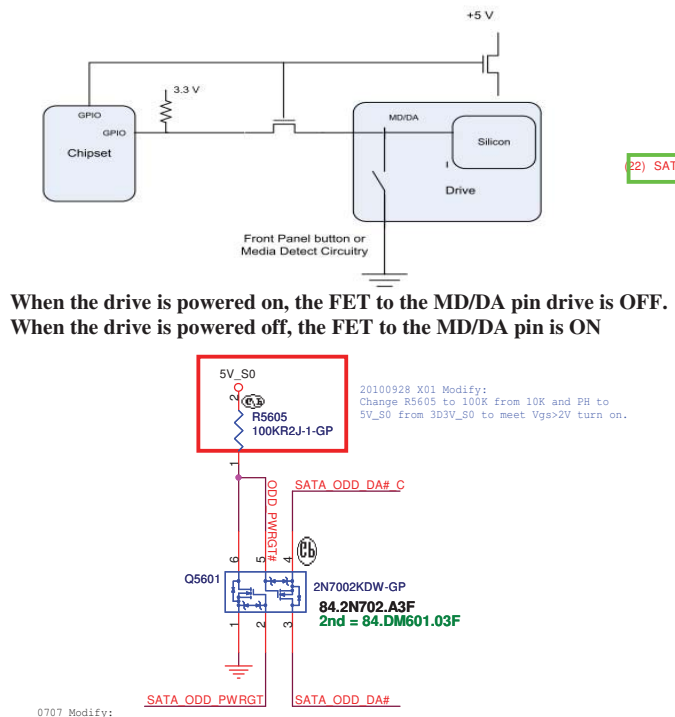


## ODD Connector



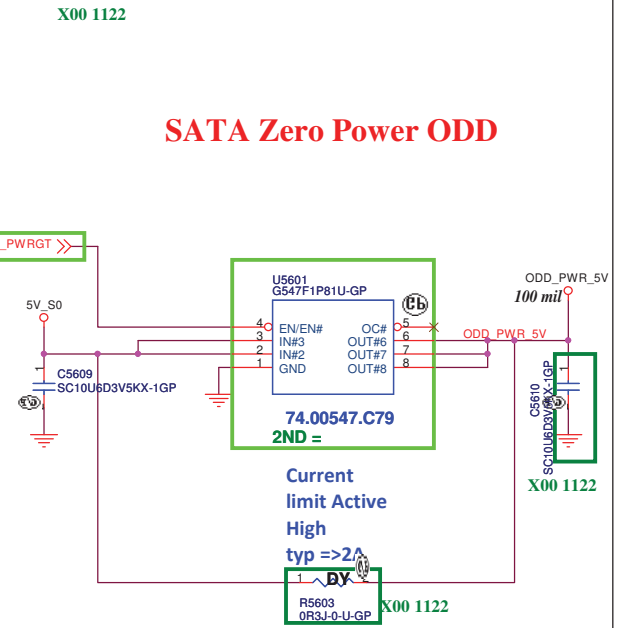
20100831 ME:  
Change ODD1 to 62.10065.221 and 2nd: 62.10065.651 to follow 20100831 connector list.  
20100902 ME:  
Change ODD1 to 62.10065.651 to follow emm file.

SUPPORT ZERO SATA ODD



When the drive is powered on, the FET to the MD/DA pin drive is OFF.  
When the drive is powered off, the FET to the MD/DA pin is ON

## SATA Zero Power ODD




<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.			
Title <b>HDD/ODD</b>			
Size A3	Document Number <b>DB13</b>	Rev <b>X00</b>	
Date: Friday, November 26, 2010		Sheet 56	of 105

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SSID = ESATA

<Core Design>



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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

*Reaserved*

Size  
A3

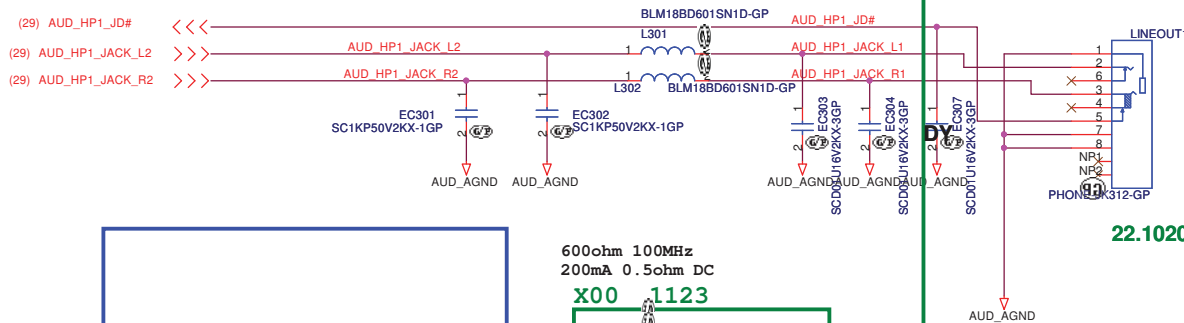
Document Number  
*DB13 DIS*

Rev  
*X00*

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SSID = AUDIO

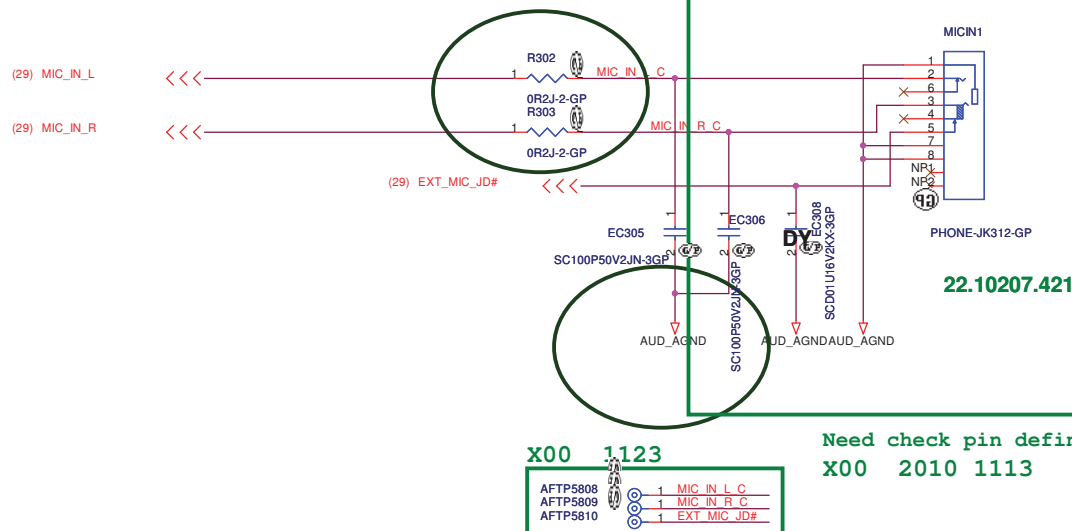
LINE1  
OUT



X00 2010 1113  
Need check pin define

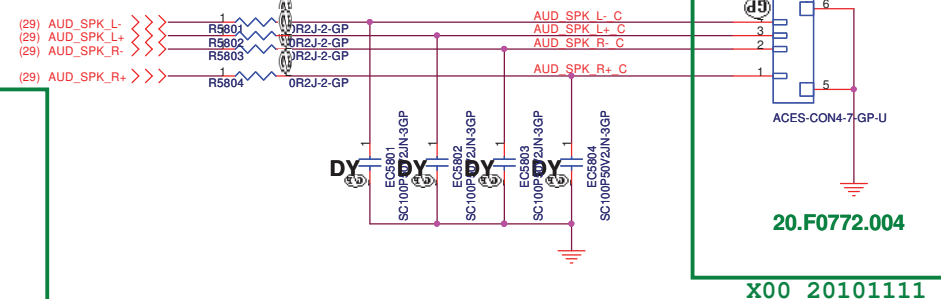
MIC IN

0916 change to  
AGND

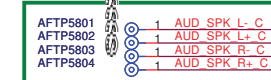


Need check pin define  
X00 2010 1113

Speaker  
Connector



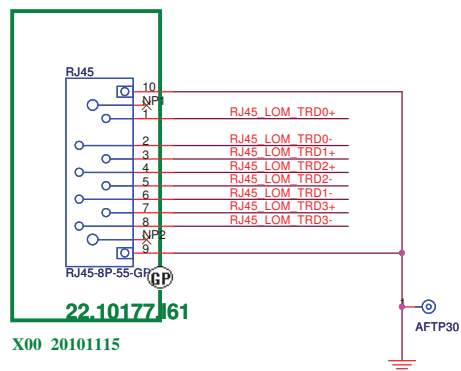
X00 1123



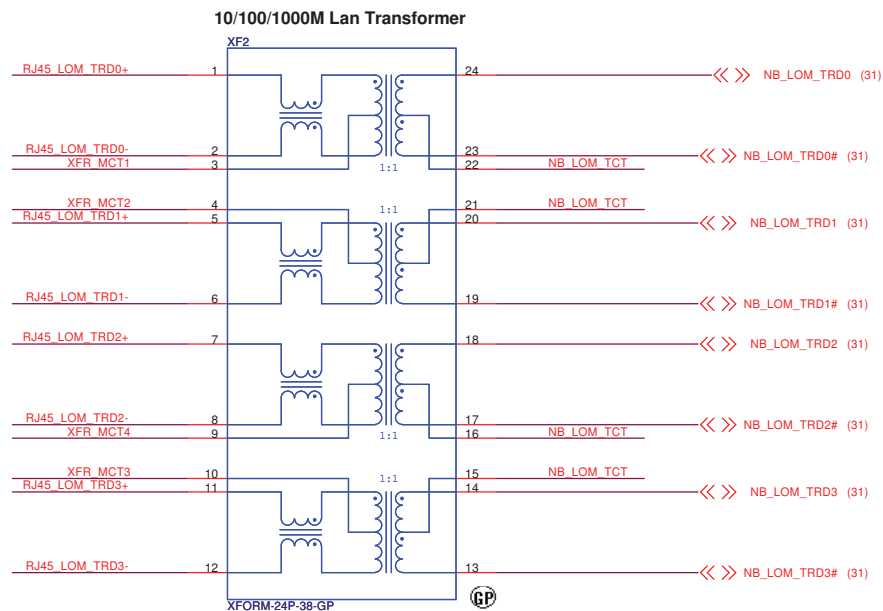
<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title <b>Audio Jack</b>			
Size A3	Document Number <b>DB13</b>	Rev <b>X00</b>	
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SSID = LOM



AFTP5901	1	RJ45 LOM TRD0+
AFTP5902	1	RJ45 LOM TRD0-
AFTP5903	1	RJ45 LOM TRD1+
AFTP5904	1	RJ45 LOM TRD2+
AFTP5905	1	RJ45 LOM TRD2-
AFTP5906	1	RJ45 LOM TRD1-
AFTP5907	1	RJ45 LOM TRD3+
AFTP5908	1	RJ45 LOM TRD3-



1st: TAIMAG 68.IH115.30A  
2nd: NETSWAP 68.69241.30C



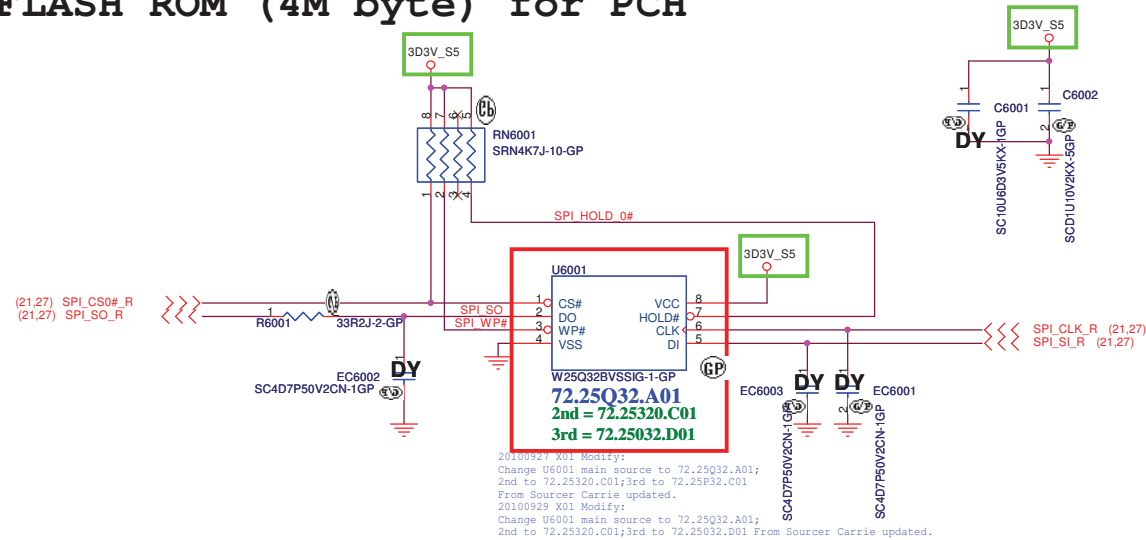
<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: <b>RJ45+ Transformer</b>			
Size: A3	Document Number: <b>DB13</b>	Rev: <b>X00</b>	
Date: Friday, November 26, 2010	Sheet: 59	of: 105	

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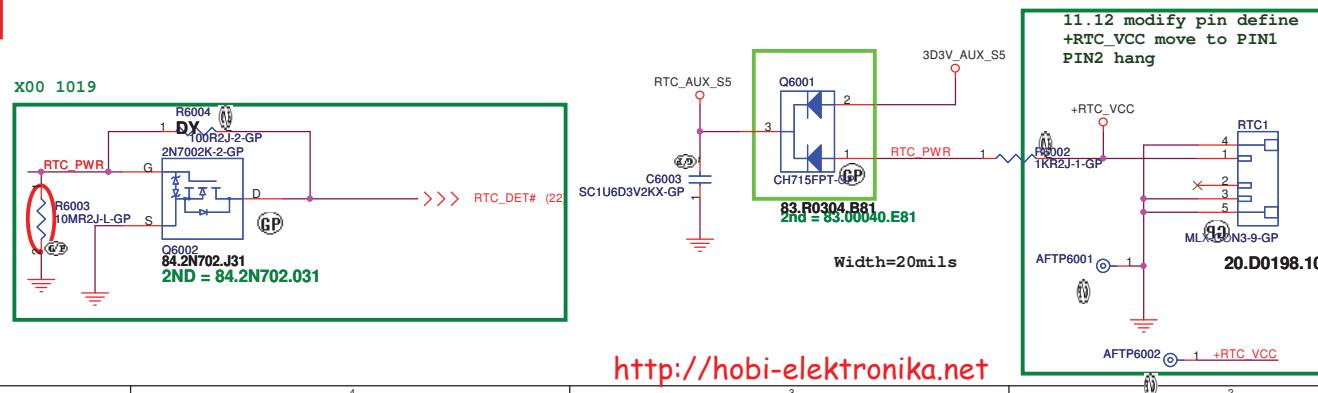
**SSID = Flash.ROM**

SPI FLASH ROM (4M byte) for PCH




	Priority	Wistron P/N	Manufacturer	Vendor P/N
X01	1	72.25Q32.A01	WINBOND	W25Q32BVSSIG
X01	2	72.25320.C01	MXIC	MX25L3206EM2L-12G
	3	72.25032.D01	SST	SST25VF032B-80-4I-S2AF
	4	72.25P32.C01	Numonyx	M25PX32-VMW6F

**SSID = RBATT**



SSID = USB

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

*Reserved*

Size

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*DB13 DIS*

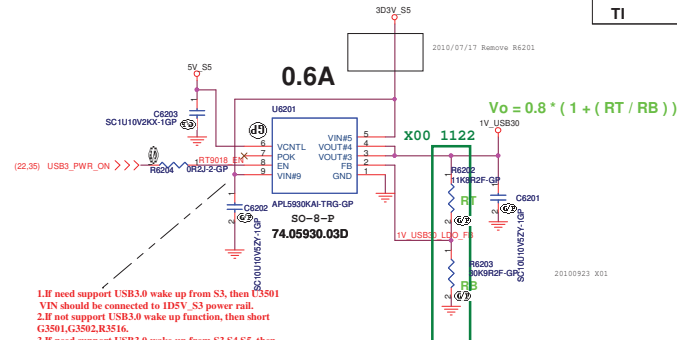
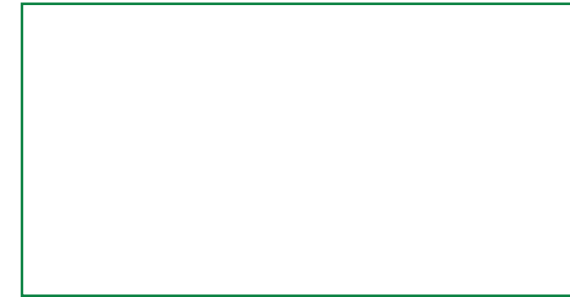
*X00*

# 1V\_USB30 LDO

2010/07/13 Move USB3.0 LDO to RB side for layout space concern

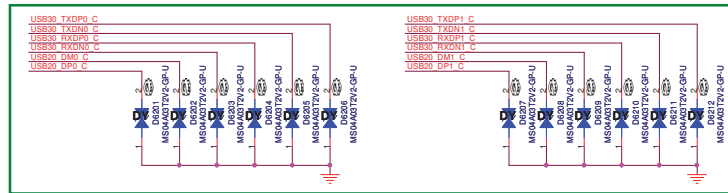
USB3.0 Host	RT (R6202)	RB (R6203)	VOUT
TI	11.8k ohm (64.11825.6DL)	30.9k ohm (64.30925.6DL)	1.1V

X00 1122 USB Charger remove

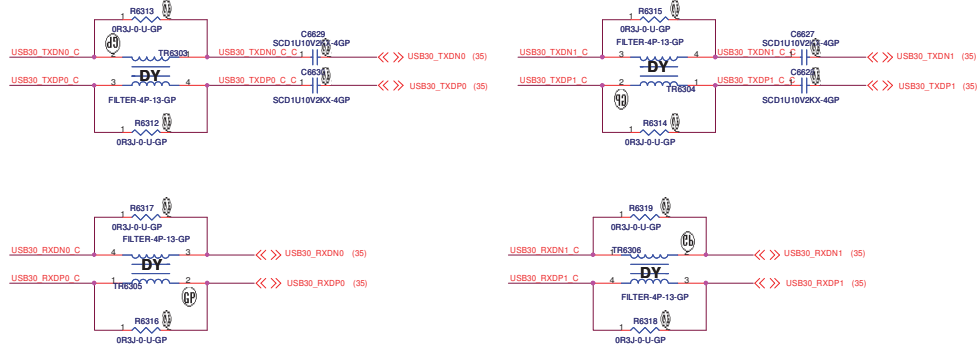
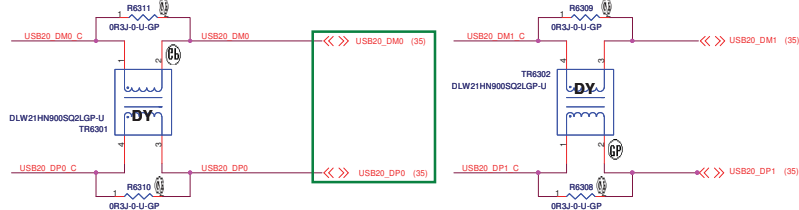


1.If need support USB3.0 wake up from S3, then U3501 VIN should be connected to ID5V\_S3 power rail.  
2.If not support USB3.0 wake up function, then short G3501,G3502,R3516.  
3.If need support USB3.0 wake up from S3,S4,S5, then U3501 VIN should be connected to 3DV\_S5 power rail.

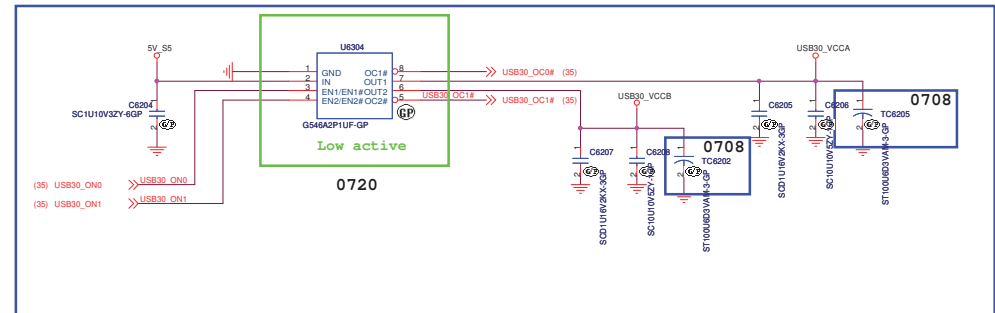
X00 1125 For TI add



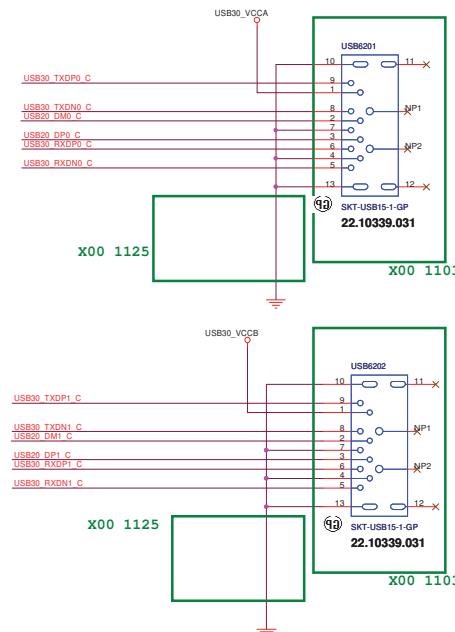
X00 1122



0701



## USB3.0 CONNECTOR




USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+ SuperSpeed RX

SSID = User.Interface

(Blanking)

<Core Design>



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Title

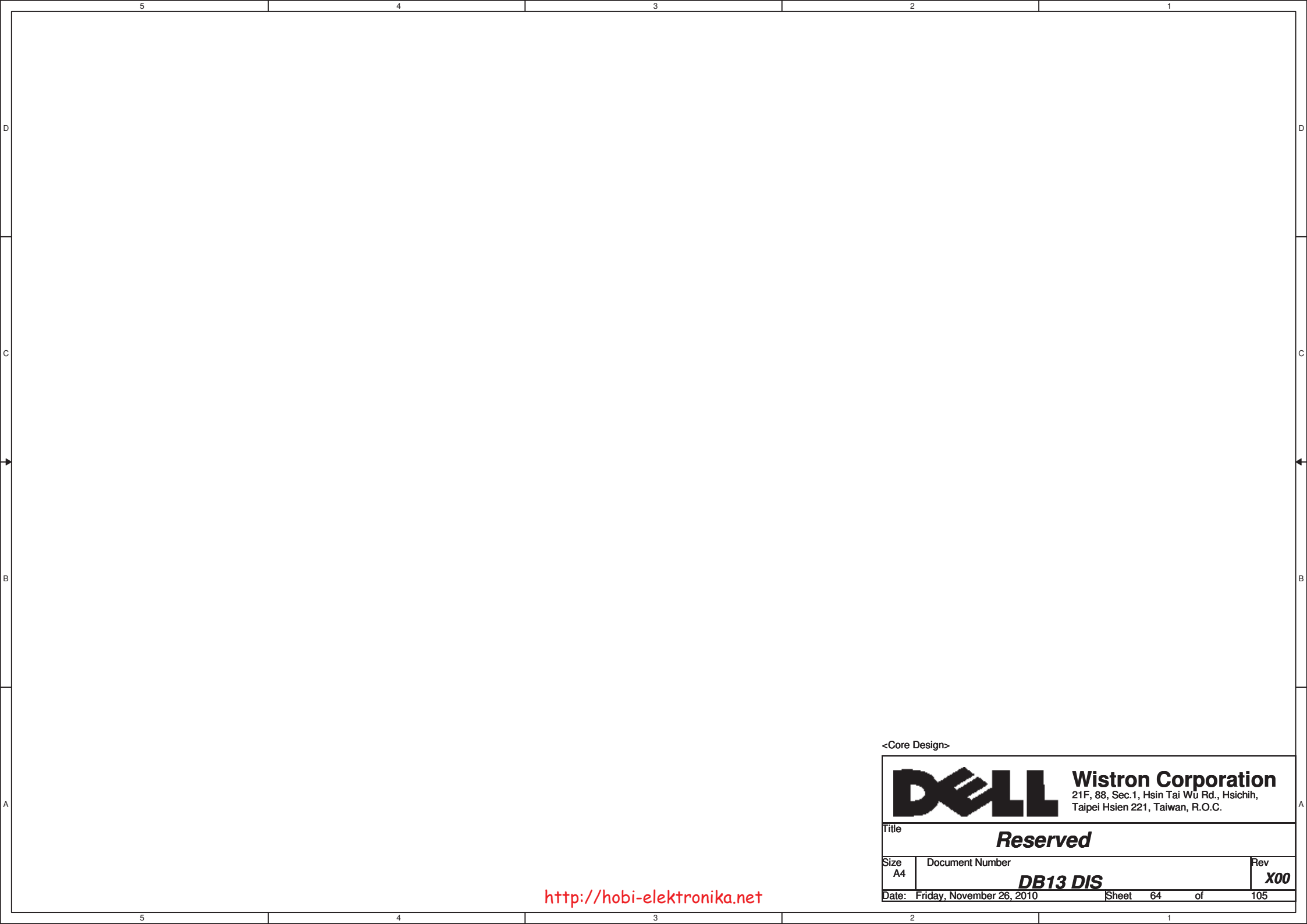
***Reserved***

Size  
A4


Document Number  
***DB13 DIS***

Rev  
***X00***

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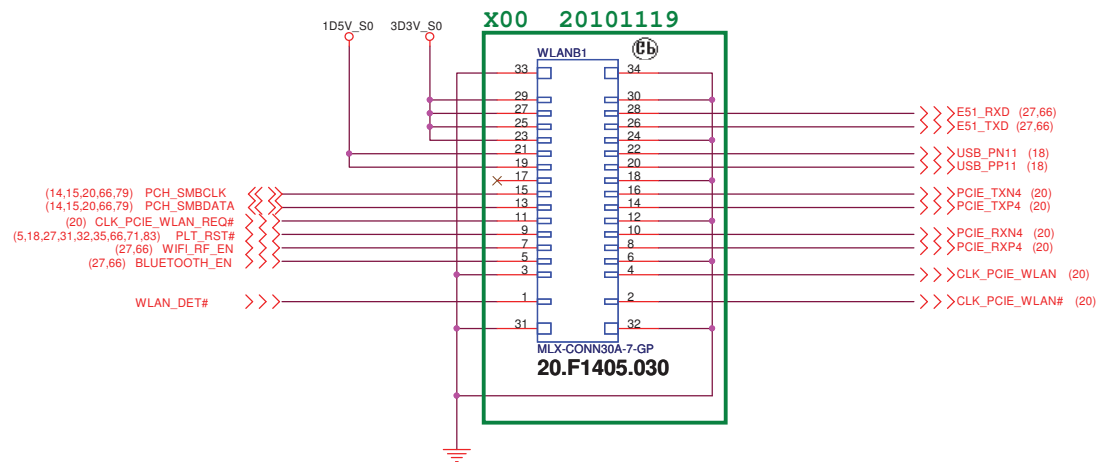


<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b><i>Reserved</i></b>		
Size A4	Document Number <b><i>DB13 DIS</i></b>	Rev <b><i>X00</i></b>
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SSID = Wireless

WWAN SMBUS  
WLAN PCIE  
WLAN PCIE  
WLAN CLK



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<Core Design>



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Title

**MINICARD(WLAN)/ITP CONN**

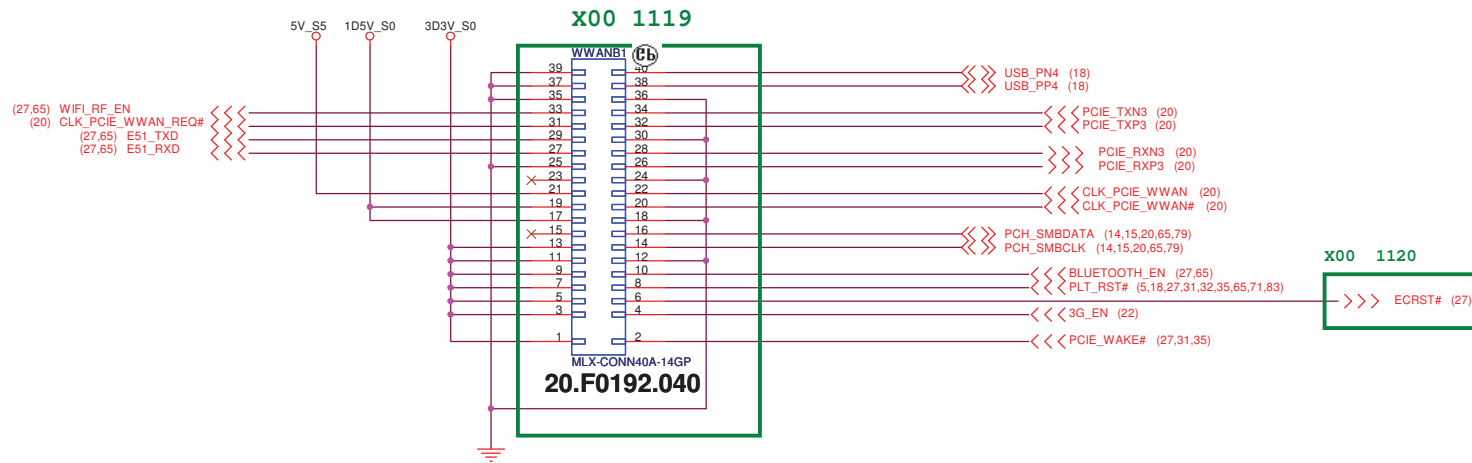
Size  
A3

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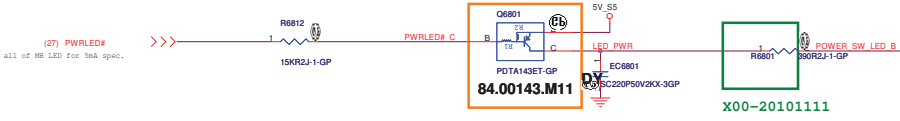
<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Reserved</b>			
Size A4	Document Number <b>DB13 DIS</b>		Rev <b>X00</b>
Date: Friday, November 26, 2010		Sheet 67 of	105

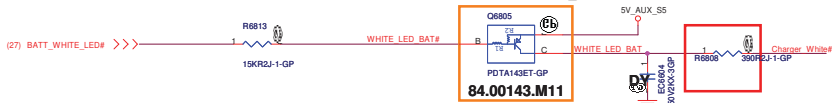
SSID = User.Interface

### Power LED(White)

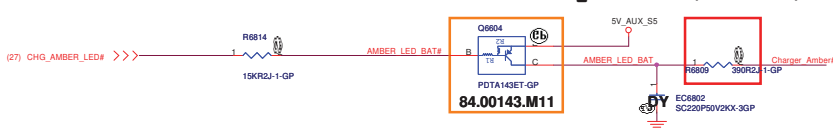
20100927 X01 Sync with the std  
Rename R6601 to R6804, rename R6604 to R6806, rename R6602 to R6808,  
rename R6608 to R6809, rename R6607 to R6810  
Change R6804, R6801, R6806, R6808, R6809, R6810, R6811 to 390 ohm to fine tune all of MB LED for 5mA spec.  
Change R6802 to 15k ohm.



### Battery LED1(White)



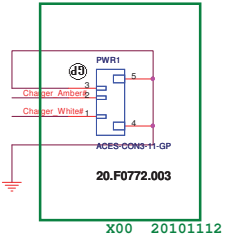
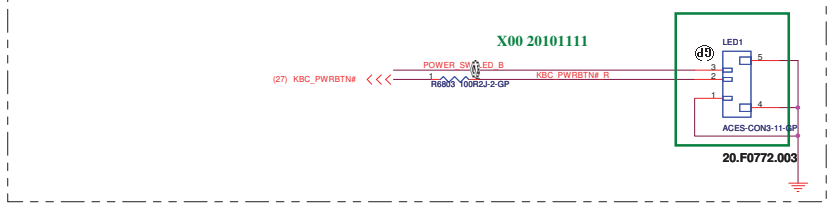
### Battery LED2 (Amber)



X00 1116 remove

X00 1116 Remove

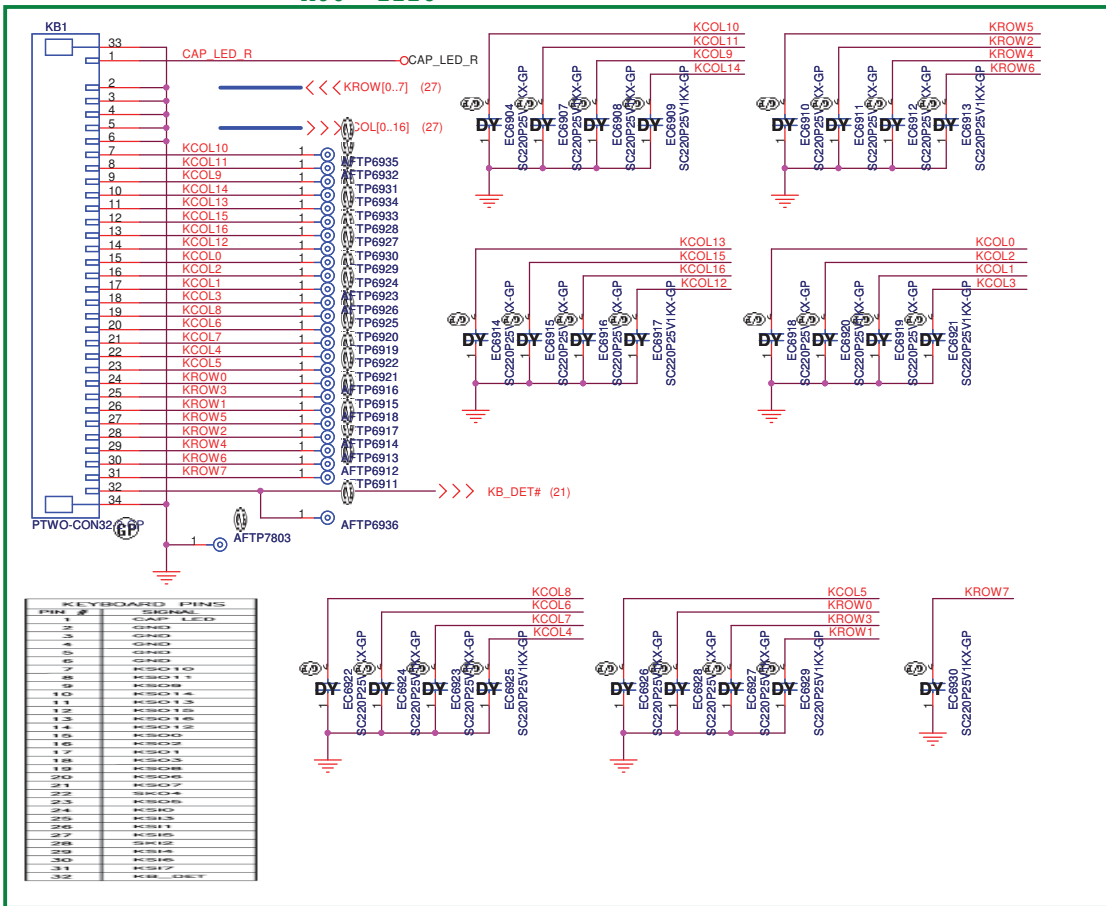
### Power button LED(White)



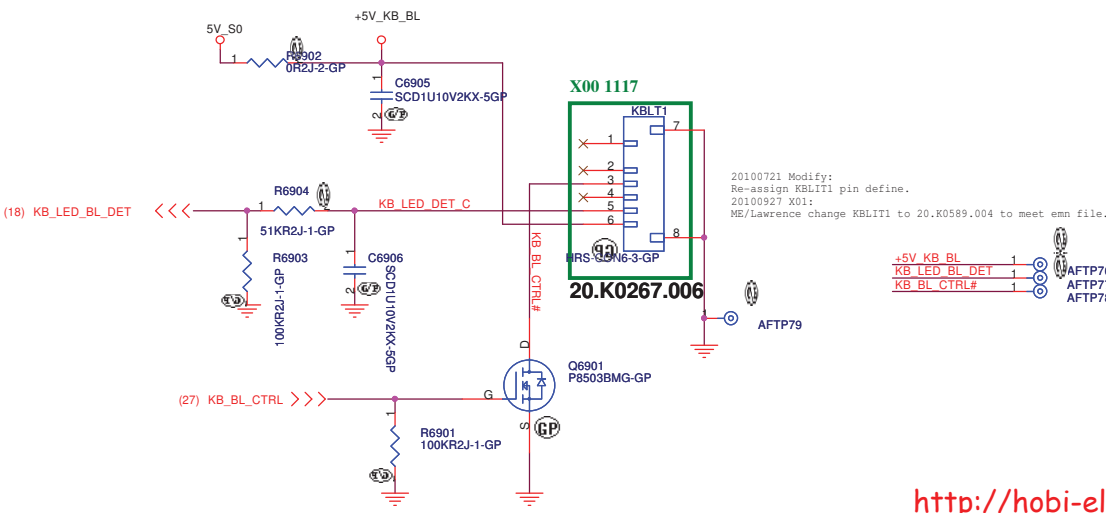
SSID = KBC

x00 1116

## Internal Keyboard Connector

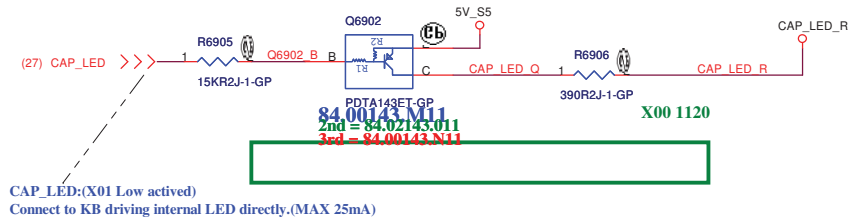


## KB Backlight Connector



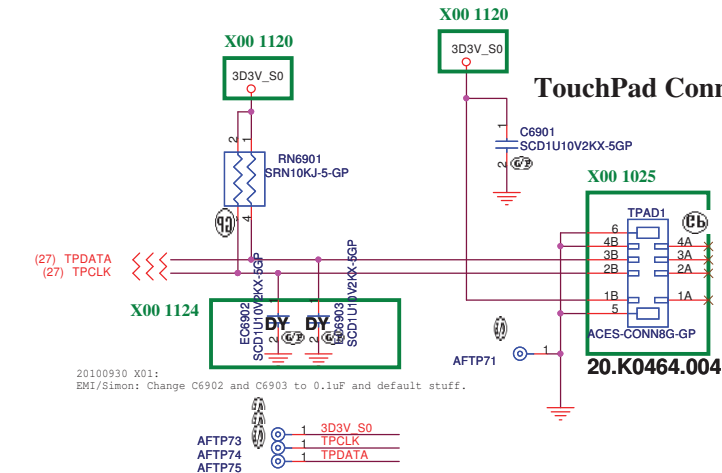
## CAP LED CONTROL

20100917 X01 Modify:  
Un-stuff R6907 and stuff Q6902,R6906  
for 5V drive CAP LED.  
20100927 X01:  
Change R6906 to 390 ohm.



CAP\_LED:(X01 Low activated)  
Connect to KB driving internal LED directly.(MAX 25mA)

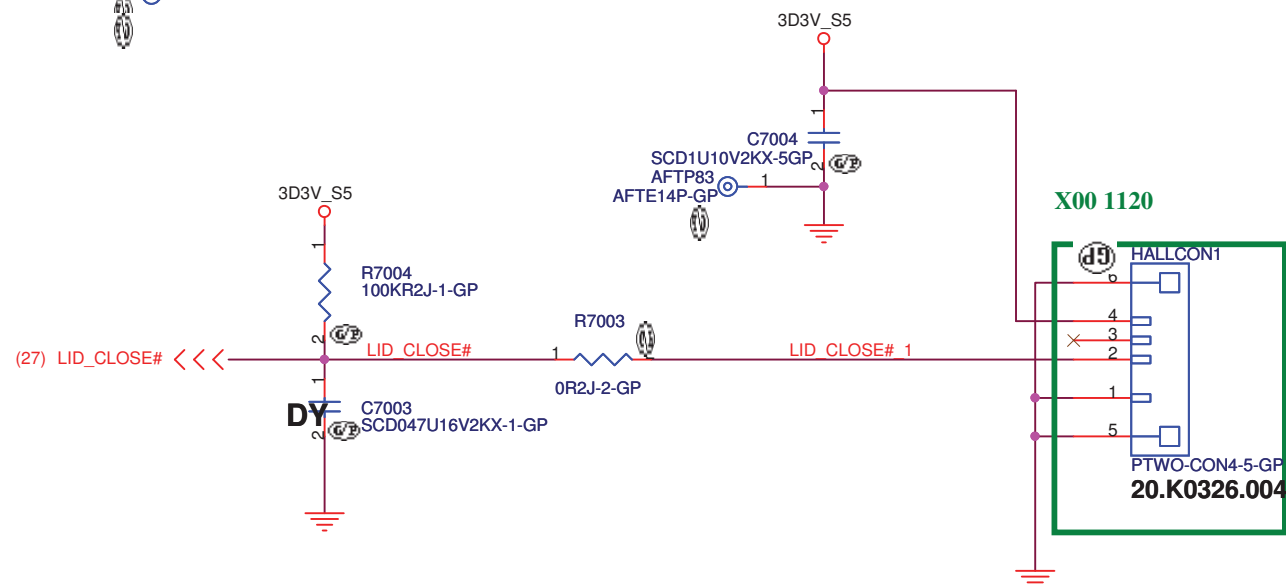
## TouchPad Connector



<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Key Board/Touch Pad/Media Board</b>			
Size A3	Document Number	Rev	
		<b>DB13 DIS</b>	
Date: Friday, November 26, 2010	Sheet 69	of	105

AFTP80 AFTE14P-GP 1 3D3V S5  
AFTP81 AFTE14P-GP 1 LID\_CLOSE# 1



<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Hall Sensor**

Size  
A4

Document Number

**DB13 DIS**

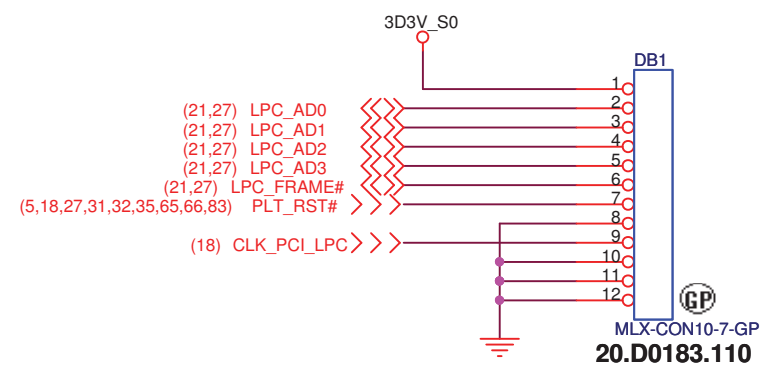
Rev

**X00**

Date: Friday, November 26, 2010

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<Core Design>



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Title

**Dubug CONN**

Size  
A4

Document Number

**DB13 DIS**

Rev  
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<Core Design>



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Title

*Reserved*

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A3	<b>DB13 DIS</b>	<b>X00</b>
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(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

A3

Document Number

**DB13 DIS**

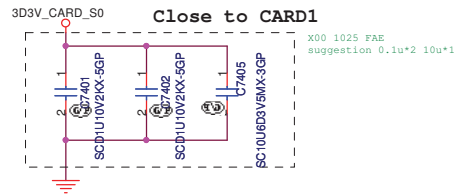
Rev

**X00**

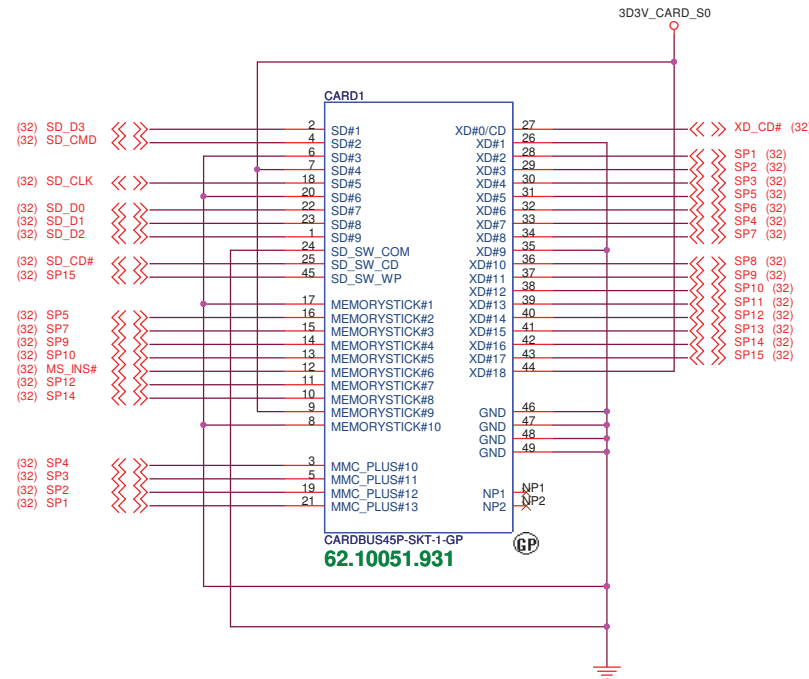
Date: Friday, November 26, 2010

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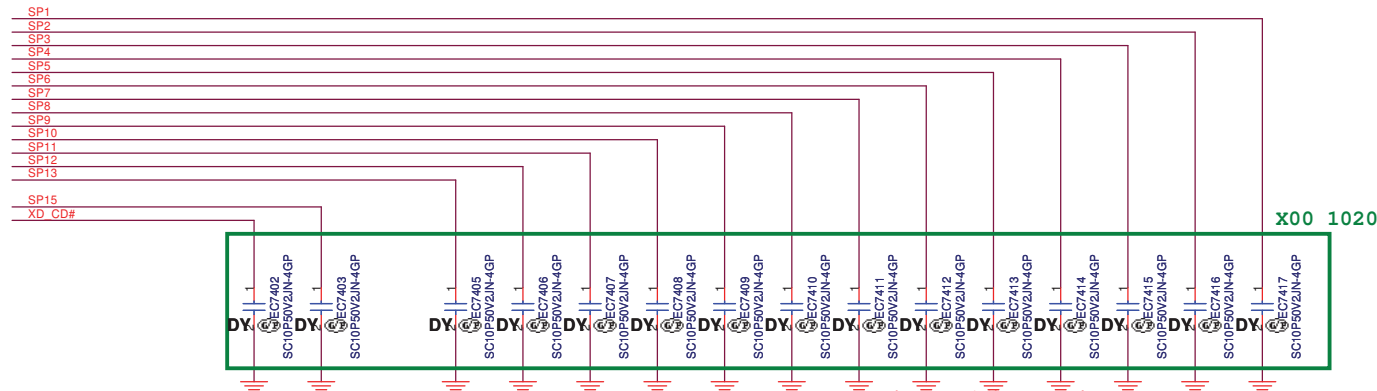
SSID = SDIO



## SD/XD/MS/MMC+ Card Reader



For EMI Reserved



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PIN	TYPE	FUNCTION	RTS5138 NET
1	SD	SD-DAT2	SP13
2	SD	SD-CD/DAT3	SP12
3	MMC_PLUS	MMC-DAT4	SP11
4	SD	SD-CMD	SP10
5	MMC_PLUS	MMC-DAT5	SP9
6	SD	SD-VSS	POWER
7	SD	SD-VDD	POWER
8	MemoryStick	MS-VSS	POWER
9	MemoryStick	MS-VCC	POWER
10	MemoryStick	MS-SCLK	SP1
11	MemoryStick	MS-DAT3	SP5
12	MemoryStick	MS-INS	SP2
13	MemoryStick	MS-DAT2	SP8
14	MemoryStick	MS-DAT0	SP9
15	MemoryStick	MS-DAT1	SP12
16	MemoryStick	MS-BE	SP14
17	MemoryStick	MS-VSS	POWER
18	SD	SD-CLK	SP8
19	MMC_PLUS	MMC-DAT6	SP7
20	SD	SD-VSS	POWER
21	MMC_PLUS	MMC-DAT7	SP5
22	SD	SD-DAT0	SP4
23	SD	SD-DAT1	SP3
24	SD	SD-COM(SW)	
25	SD	SD-CD(SW)	SP6
26	XD	XD-GND	POWER
27	XD	XD-CD	XD_CD#
28	XD	XD-R/B	SP1
29	XD	XD-RE	SP2
30	XD	XD-CE	SP3
31	XD	XD-CLE	SP4
32	XD	XD-ALE	SP5
33	XD	XD-WE	SP6
34	XD	XD-WP	SP7
35	XD	XD-GND	POWER
36	XD	XD-D0	SP8
37	XD	XD-D1	SP9
38	XD	XD-D2	SP10
39	XD	XD-D3	SP11
40	XD	XD-D4	SP12
41	XD	XD-D5	SP13
42	XD	XD-D6	SP14
43	XD	XD-D7	XD-D7
44	XD	XD-VCC	POWER
45	SD	SD-WP(SW)	SP1


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Title			<b>CARD Reader CONN</b>	
Size	Document Number	Rev		
A3	<b>DB13</b>	<b>X00</b>		
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Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

For ADI G-sensor : R7901 is required.  
For ST G-sensor : R7901 need DY

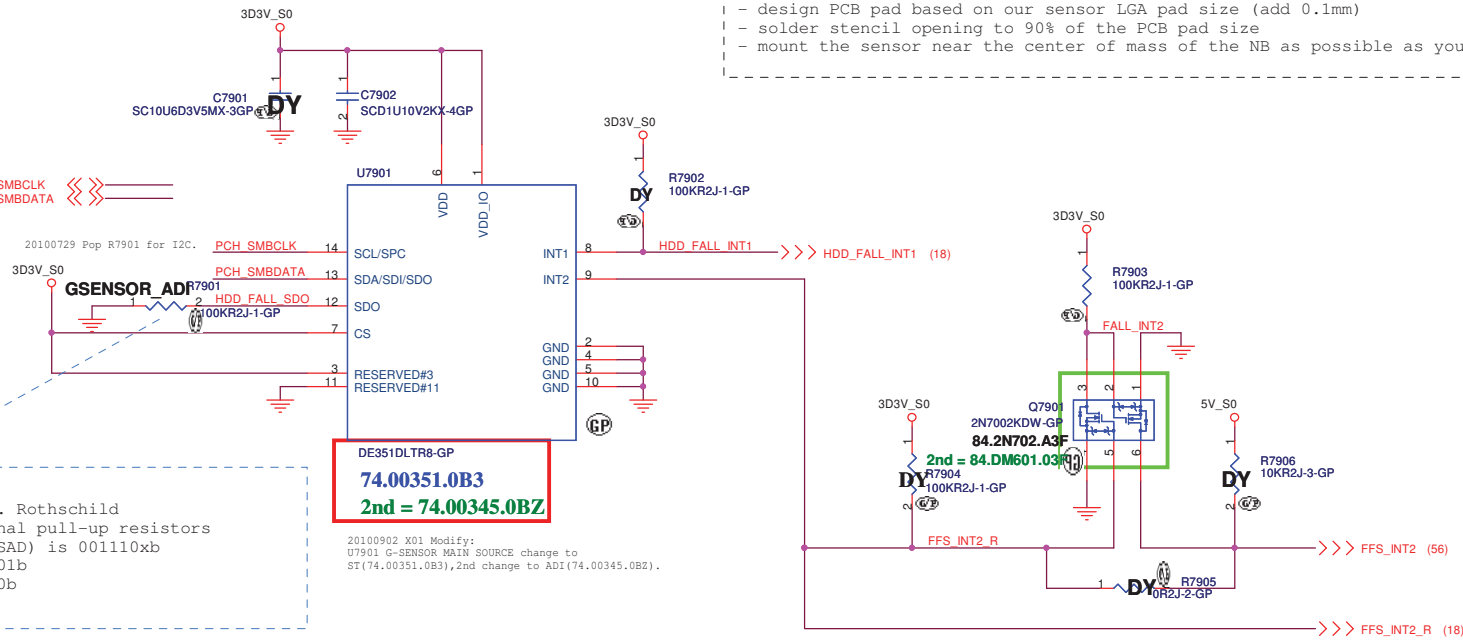
09/0422  
(#1) Just pull +3.3V\_RUN ~ Ref. Rothschild  
(#2) FAE/ DY is ok, chip internal pull-up resistors  
(#3) From spec, Slave Address(SAD) is 001110xb  
Pull HIGH SAD is 0011101b  
Pull GND SAD is 0011100b

DE351DLTR8-GP  
74.00351.0B3  
2nd = 74.00345.0BZ

20100902 X01 Modify:  
U7901 G-SENSOR MAIN SOURCE change to  
ST(74.00351.0B3), 2nd change to ADI(74.00345.0B2).


Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.



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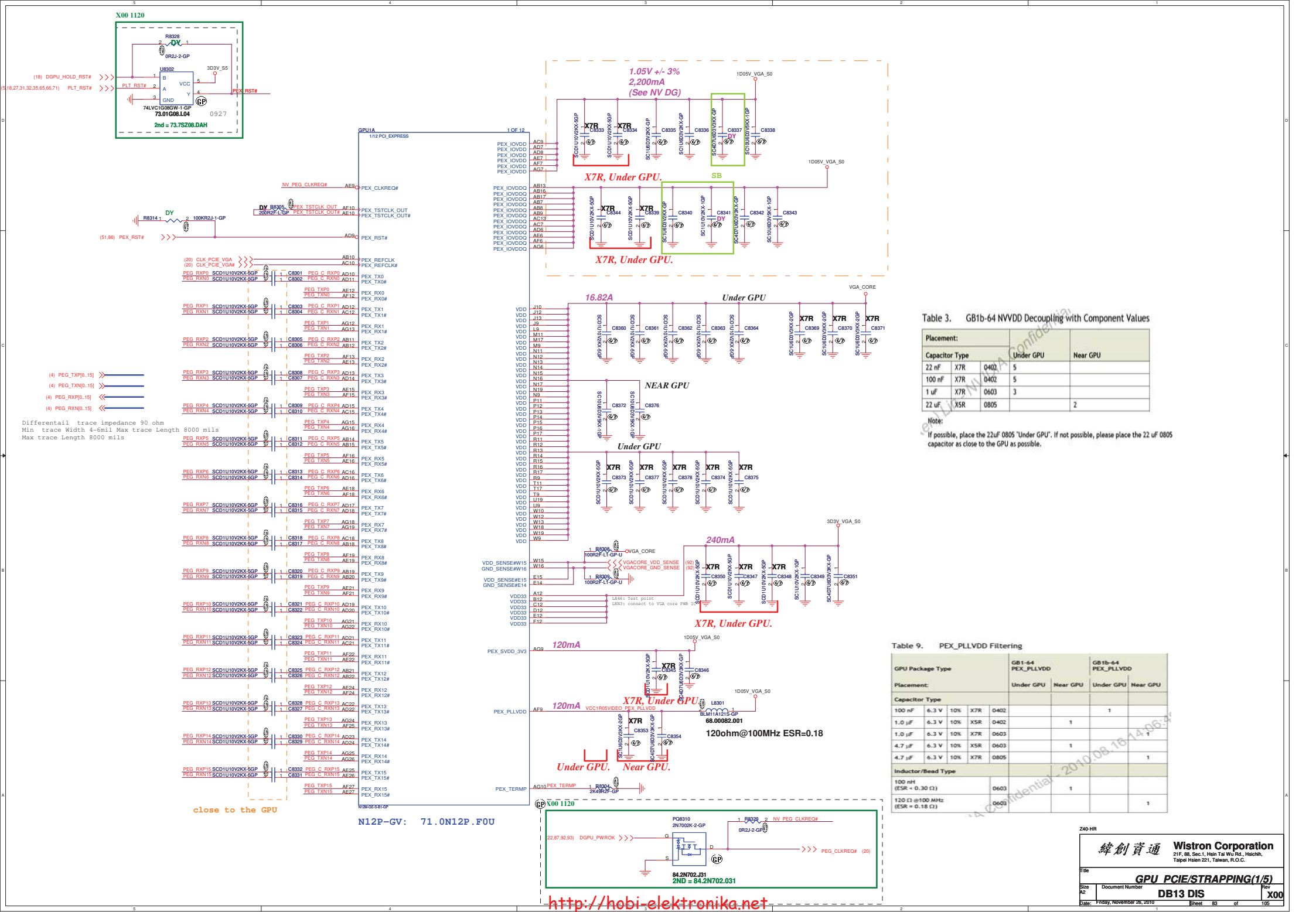
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***IO Board Connector***

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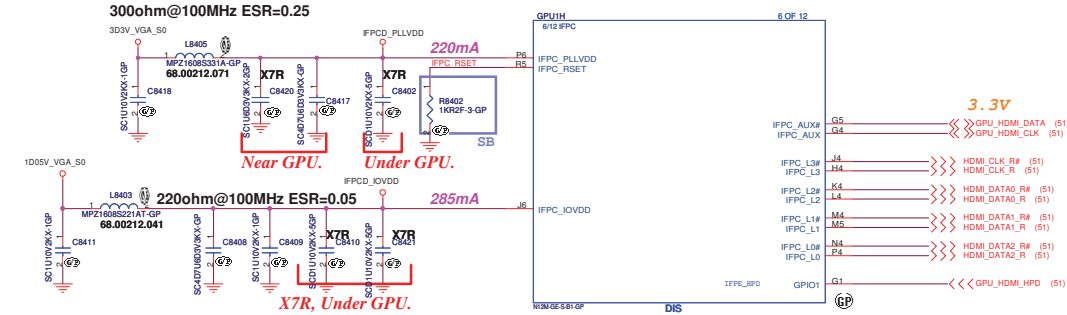


If a DAC interface is not required, it should be disabled by:  
1. Adding a pull-down to the DAC\_VDD with a 10 kilohm resistor to GND.  
2. All other DAC I/O pins can be left floating.

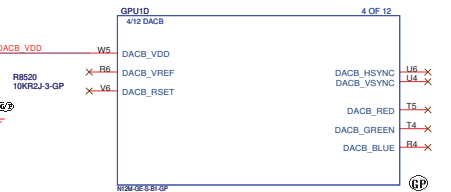
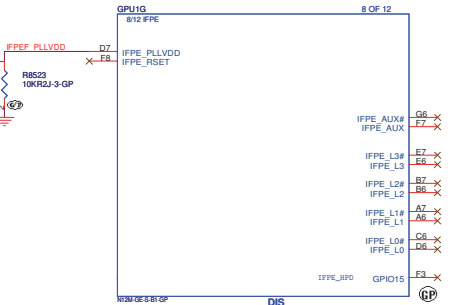
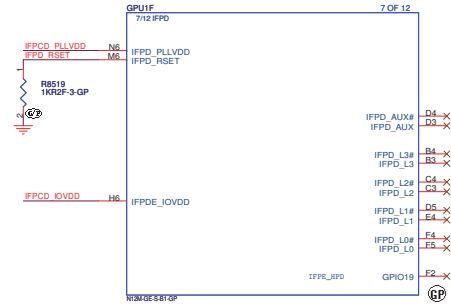
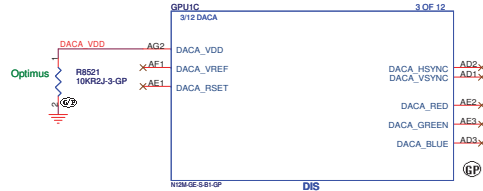
In Optimus mode the GPU does not drive certain interfaces. These interfaces should be treated as unused and appropriate terminations per the GPU design guide should be applied to the signal or the power supply block.

The following guidelines only apply to a fully unused IFP macro:

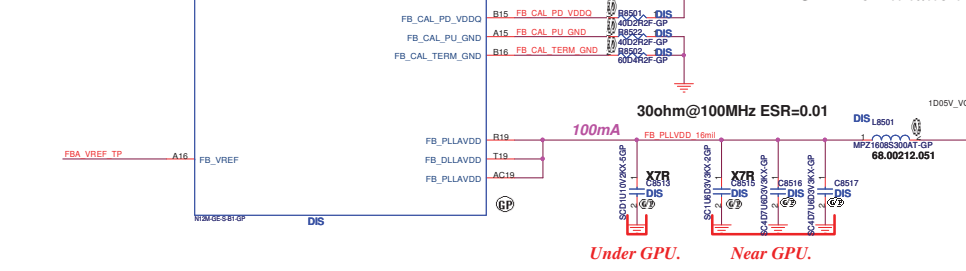
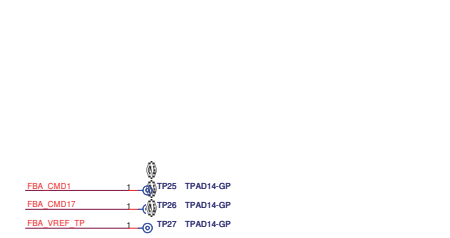
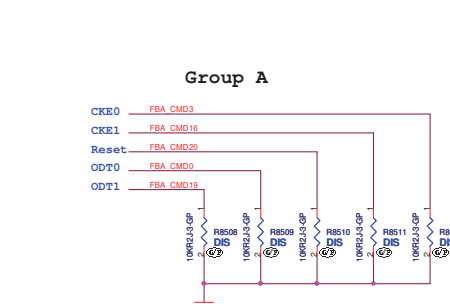
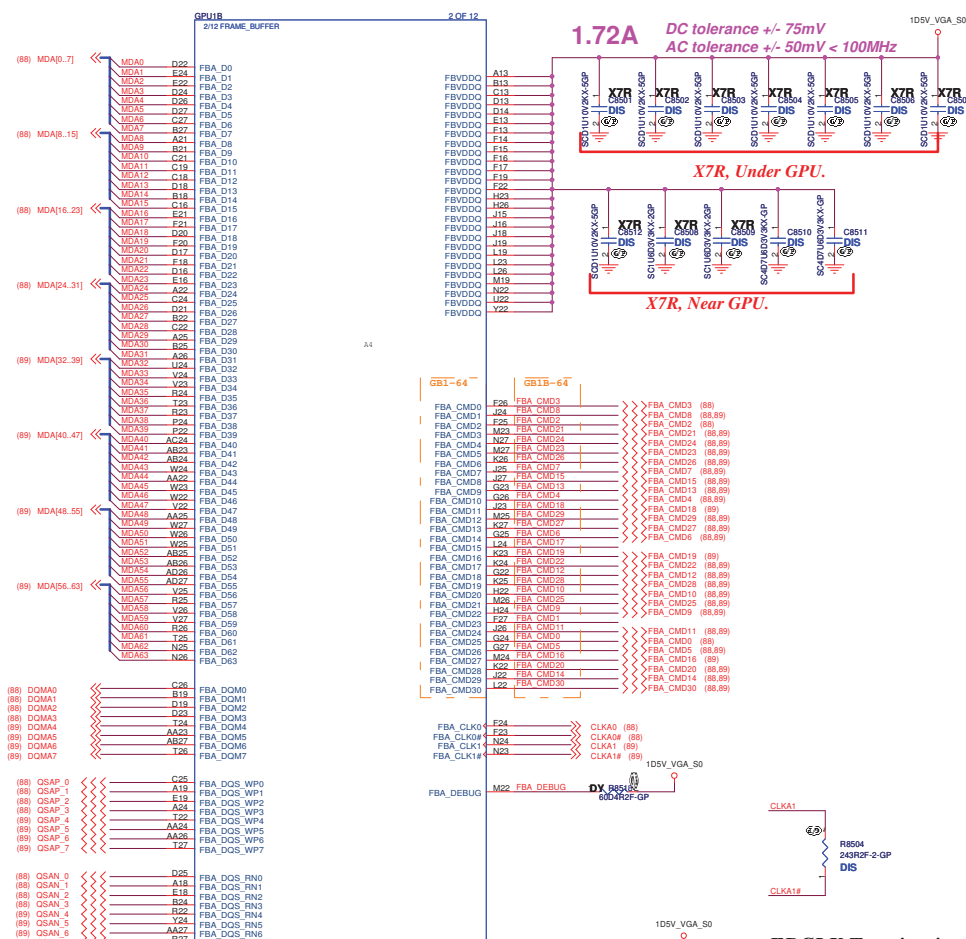
- 1. Pull down IFPxy\_IOVDD with 10 kilohm resistor.
- 2. Pull down IFPxy\_PLLVDD with 10 kilohm resistor.
- 3. The other IO pins can be NC; this includes unused data lines.



If either IFPC or IFPD is used, then the whole IFPCD interface is considered as being used. This is because IFPC and IFPD share one macro design so one IO interface cannot be independently disabled.



If either IFPC or IFPD is used, then the whole IFPCD interface is considered as being used. This is because IFPC and IFPD share one macro design so one IO interface cannot be independently disabled.



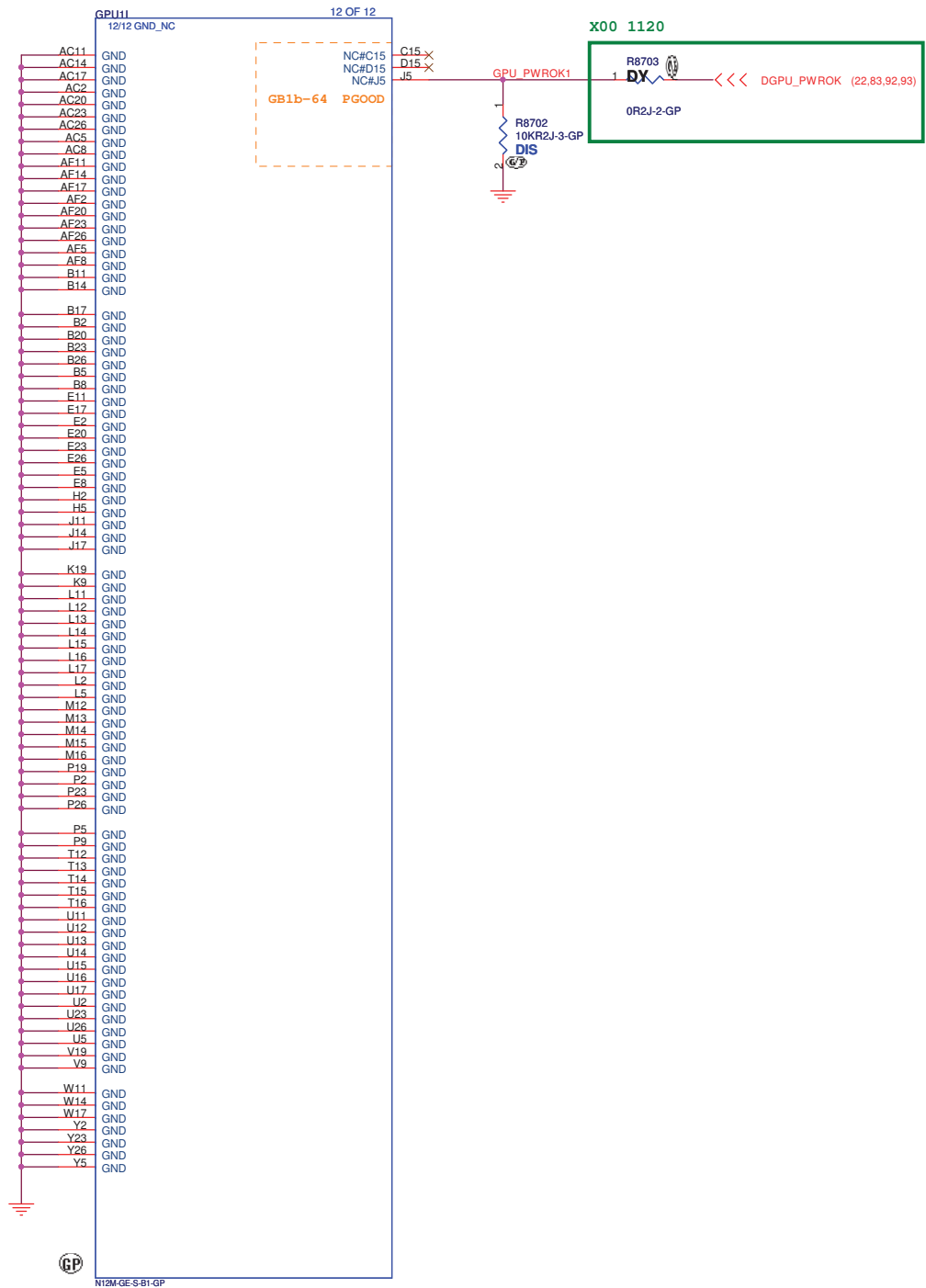
FBCLK Termination place on VRAM side

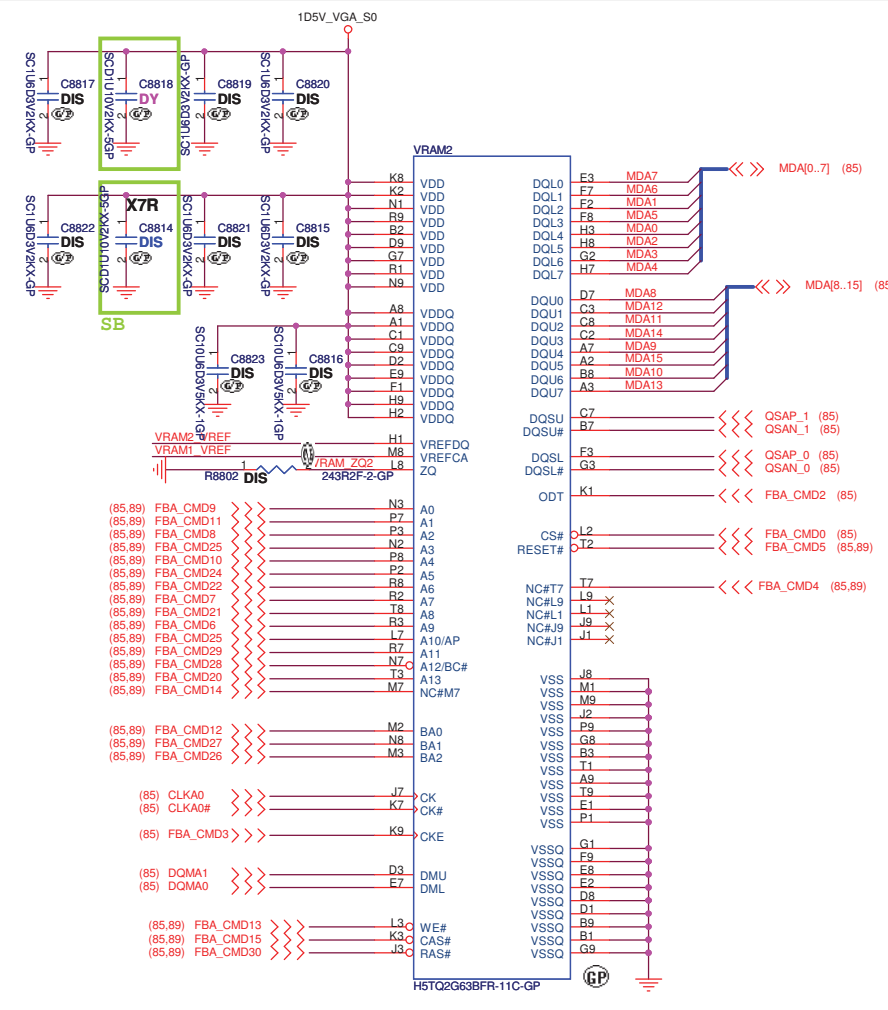
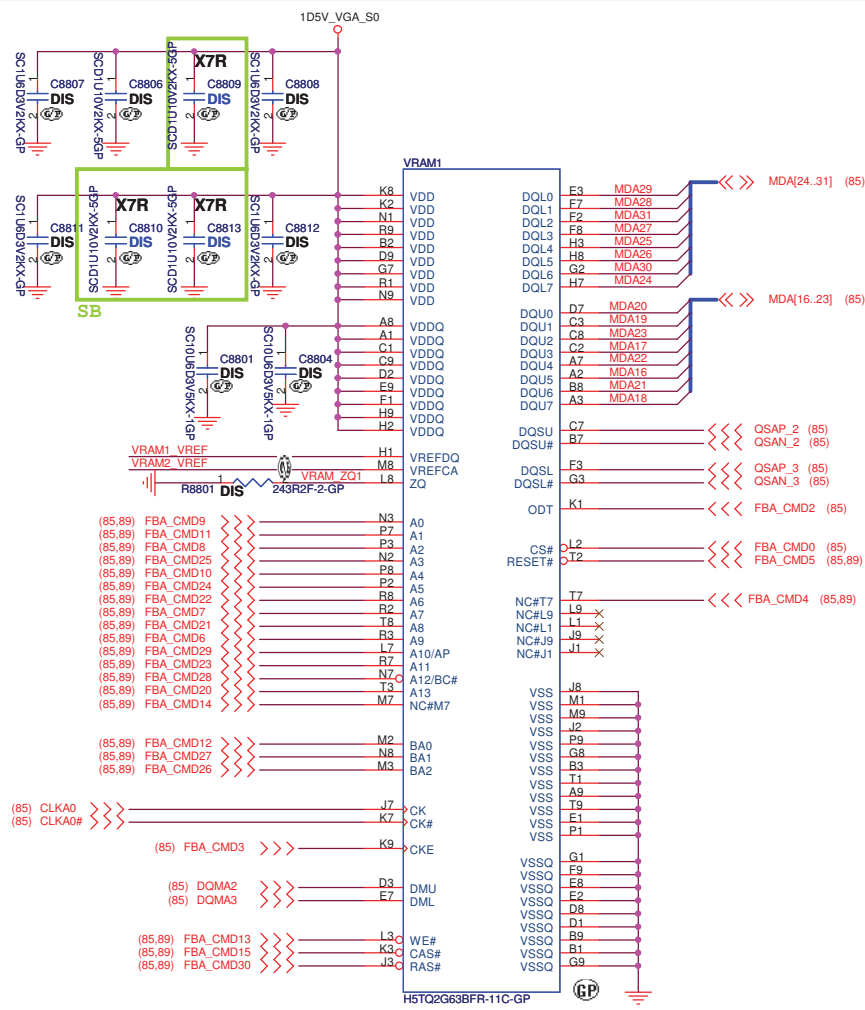


Table 4. FB\_PLLAVDD and FB\_DLLAVDD Filtering

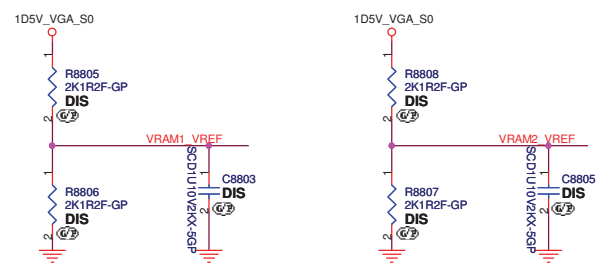
GPU Package Type	GB1-64 FB_PLLAVDD and FB_DLLAVDD Combined		GB1b-64 FB_PLLAVDD and FB_DLLAVDD Combined	
	Under GPU	Near GPU	Under GPU	Near GPU
Placement:				
Capacitor Type				
100 nF 6.3 V 10% X7R 0402			1	
1.0 uF 6.3 V 10% X5R 0402		1		
1.0 uF 6.3 V 10% X7R 0603				1
4.7 uF 6.3 V 10% X5R 0603		1		
10 uF 6.3 V 10% X7R 0805				1
Bead Type				
300 Ω @100 MHz (ESR = 0.25 Ω)	0603	1		
30 Ω @100 MHz (ESR = 0.01 Ω)	0603			1

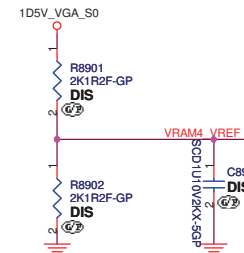
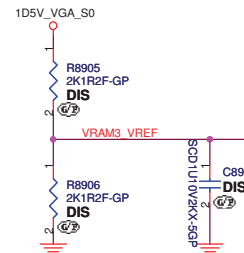
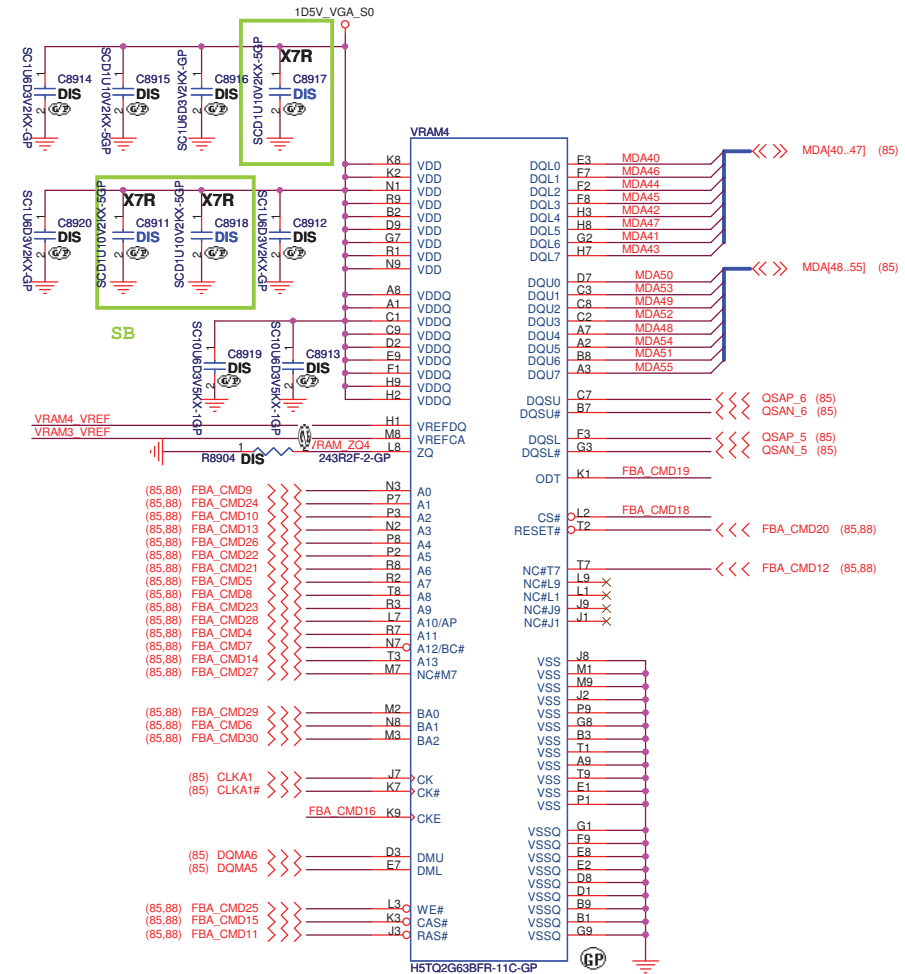
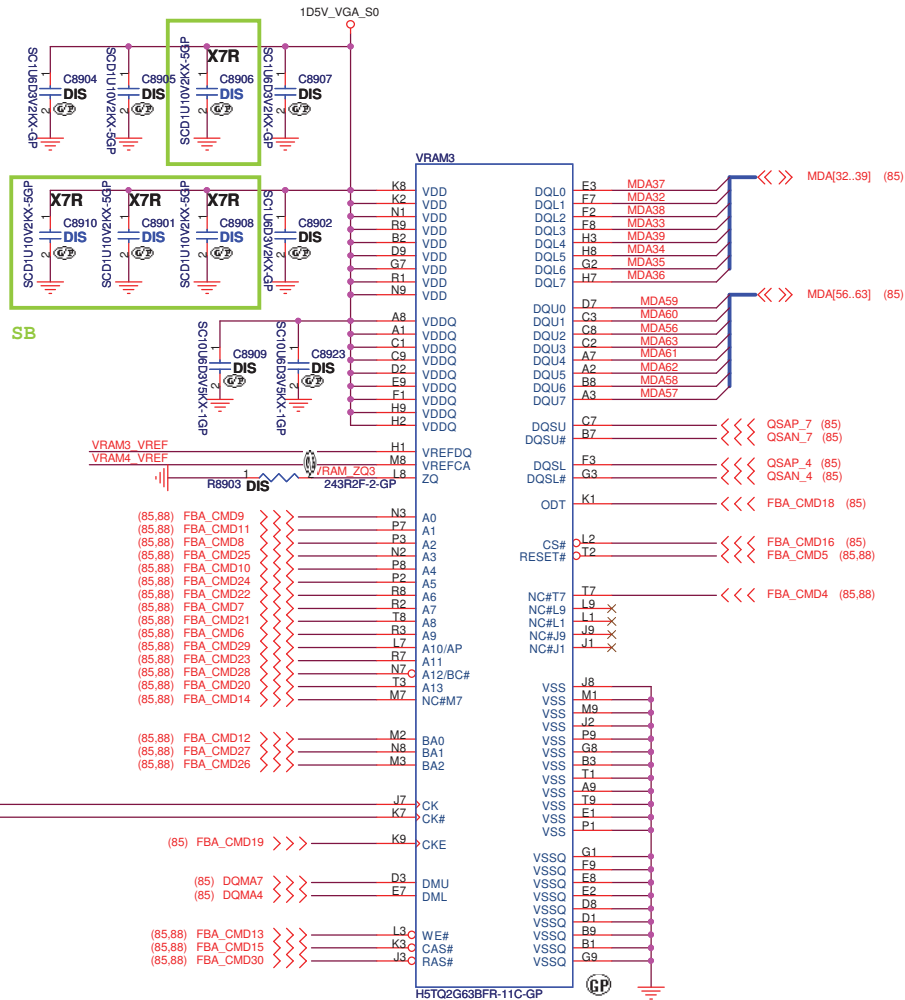






72.41646.Q0U K4W1G1646G-BC11 Samsung 1Gb  
 72.42164.D0U K4W2G1646C-HC11 Samsung 2Gb  
 72.51G63.H0U H5TQ1G63DFR-11C Hynix 1Gb  
 72.52G63.A0U H5TQ2G63BFR-11C Hynix 2Gb






72.41646.Q0U K4W1G1646G-BC11 Samsung 1Gb  
 72.42164.D0U K4W2G1646C-HC11 Samsung 2Gb  
 72.51G63.H0U H5TQ1G63DFR-11C Hynix 1Gb  
 72.52G63.A0U H5TQ2G63BFR-11C Hynix 2Gb



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Size  
A2

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X00

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DB13 DIS

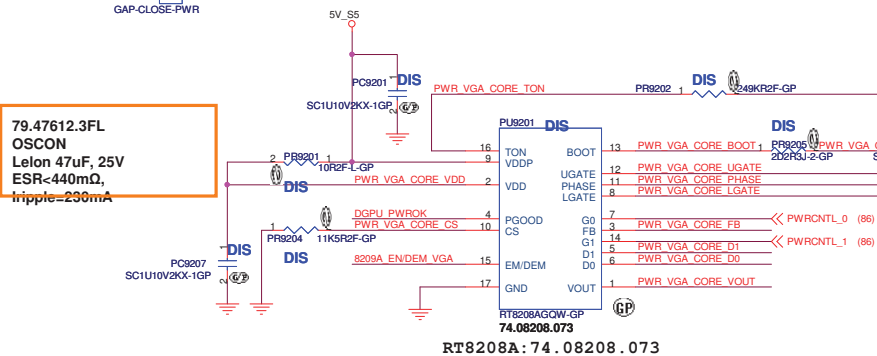
Date: Friday, November 26, 2010

Rev  
X00

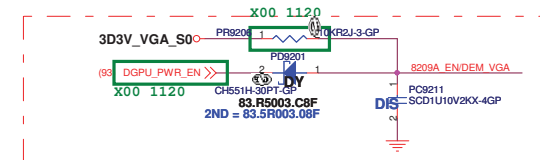
Sheet 91 of 105

**SSID = PWR.Plane.Regulator\_GFX**

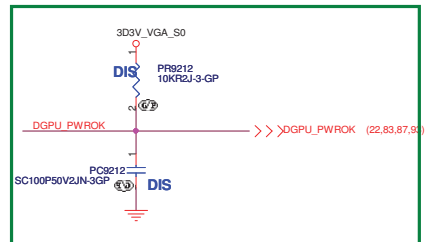
79.47612.3FL  
OSCON  
Lelon 47uF, 25V  
ESR<440mΩ,  
tripple=230mA



RT8208A: 74.08208.073



X00 1120



N12M-GS2/N12P-GV ES

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8	L	L	0.925V

Memory clock: 324MHz

Engine clock: 405MHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J  
O/P cap: 330U 2V EEF5X0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01  
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037  
L/S: SI7460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

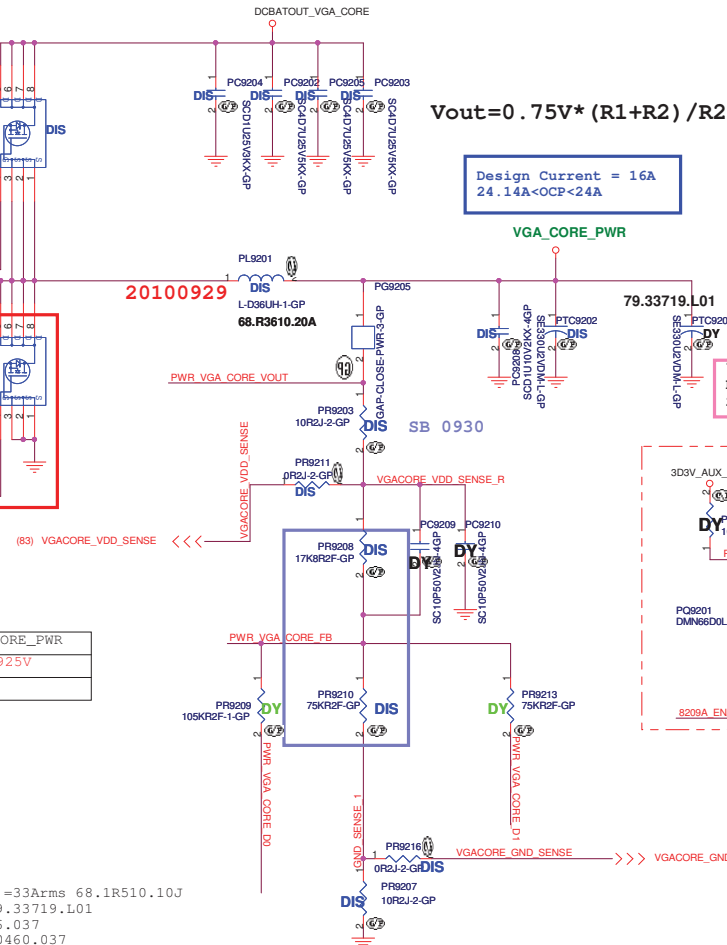
Switching freq-->350KHz

Frequency setting

470K -->165KHz

200K -->323KHz

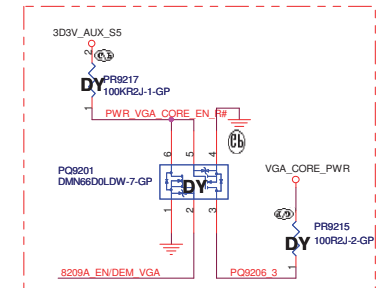
100K -->500KHz



Vout=0.75V\* (R1+R2) / R2

Design Current = 16A  
24.14A<OCP<24A

79.33719.L01  
Panasonic cap 330uF  
2V, ESR=9mohm



Z40-HR

緯創資通		Wistron Corporation	
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Title: RT8208A +VGA CORE			
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Title			<b>Reserved</b>		
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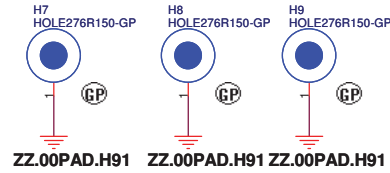
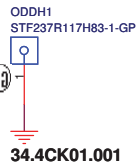
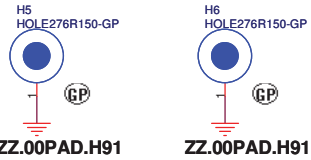
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Title

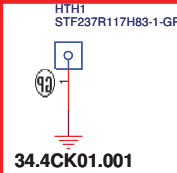
*Reserved*

Size	Document Number	Rev
A3	<b>DB13 DIS</b>	<b>X00</b>
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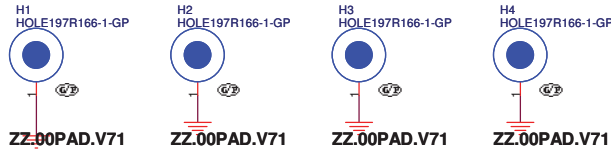
## X00 1111 Change to ZZ.00PAD.H91



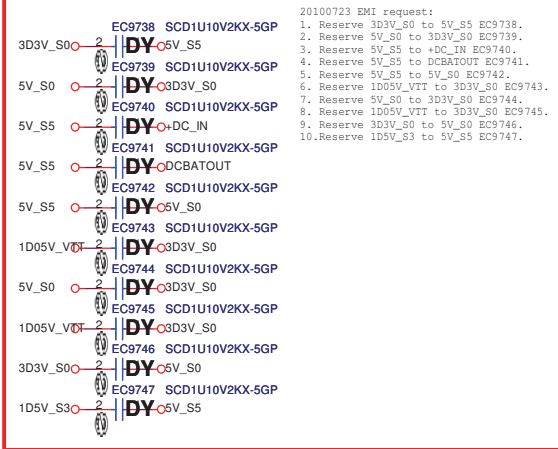
## X00 1111 Add 34.4CK01.001



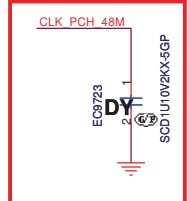
20100913 Change H11~H13 to ZZ.00PAD.V71 from ME/Lawrence updated latest DXF&EMN on X01.



## EMI Request

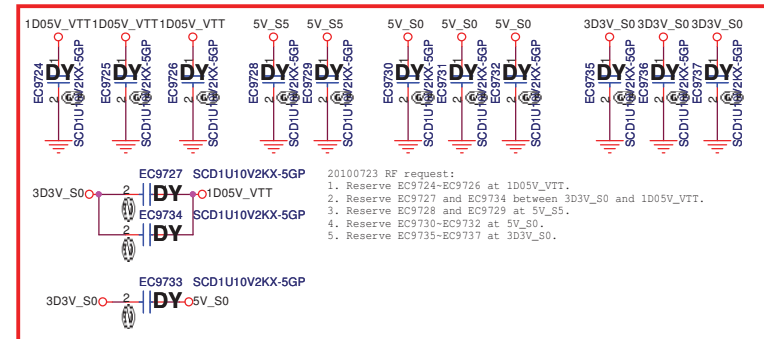


2010/07/14 EMI request  
2010/07/21 rename C3205 to EC9723



(20) CLK\_PCH\_48M >>>

## RF Request



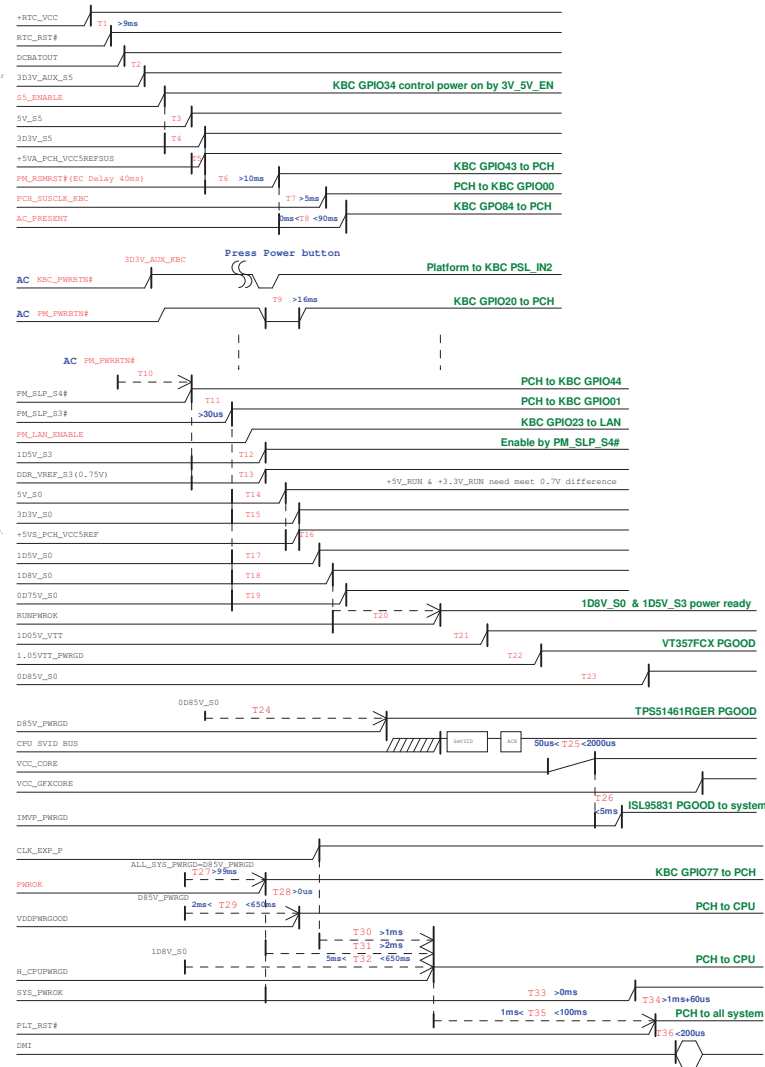
<Core Design>

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Title			
<b>UNUSED PARTS/EMI Capacitors</b>			
Size	Document Number		Rev
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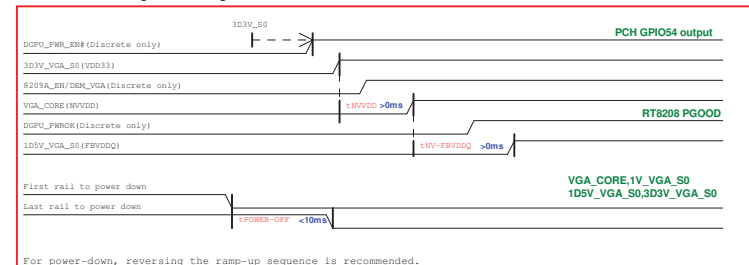
# Huron River Platform Power Sequence

## (AC mode)

red word: KBC GPIO

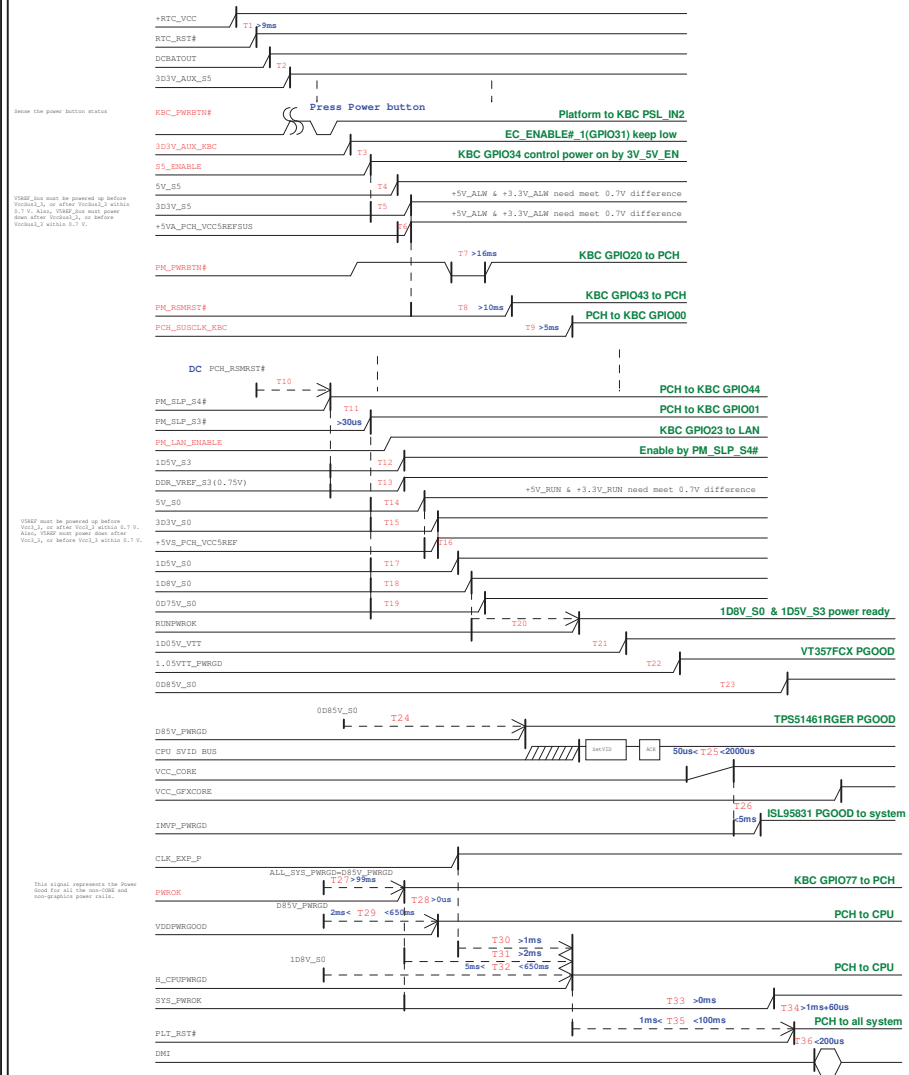


### N12P-GV Power-Up/Down Sequence



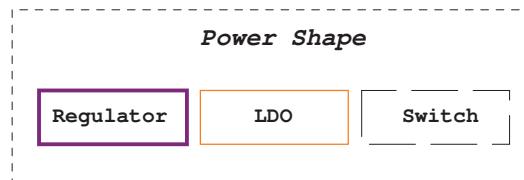
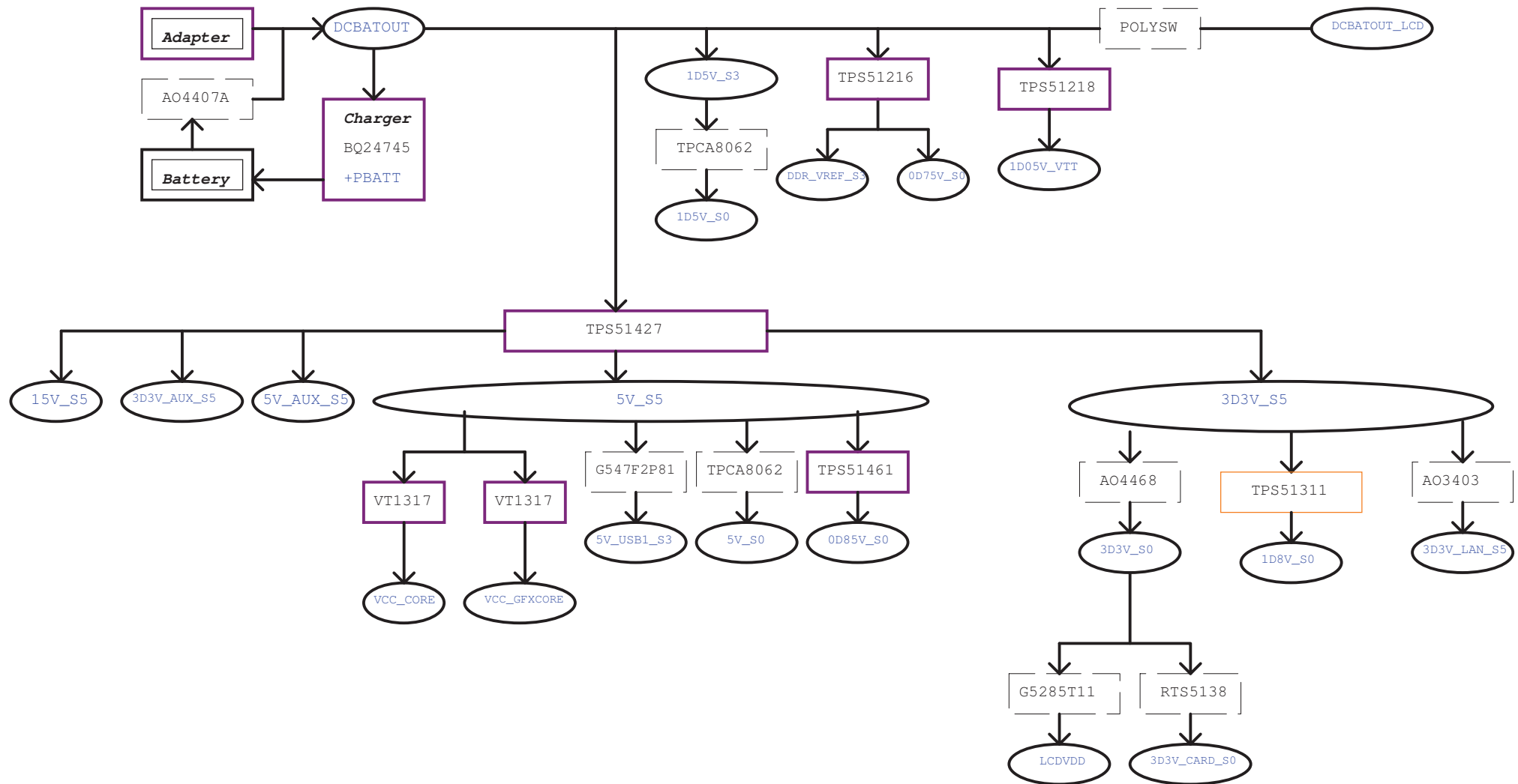
## (DC mode)

red word: KBC GPIO

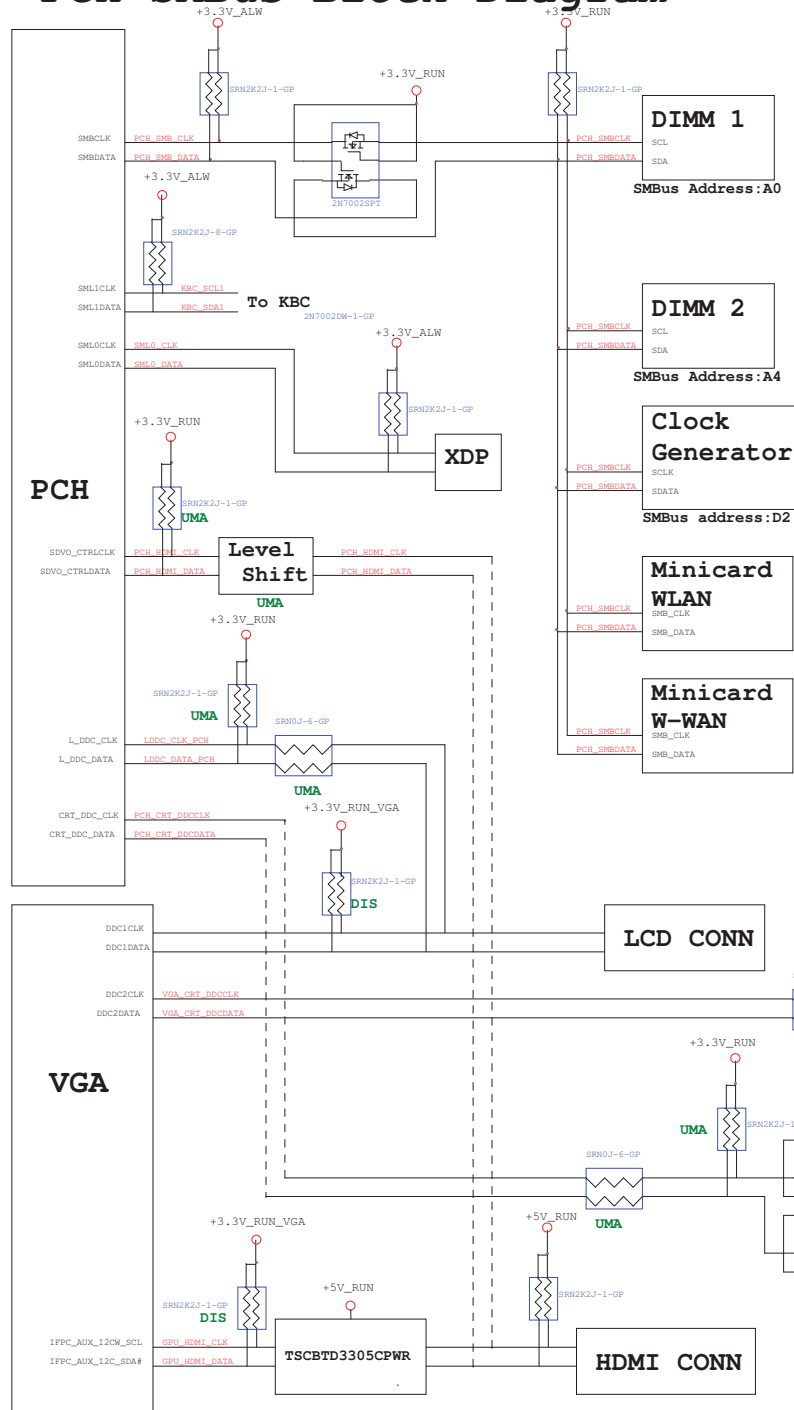


<http://hobi-elektronika.net>

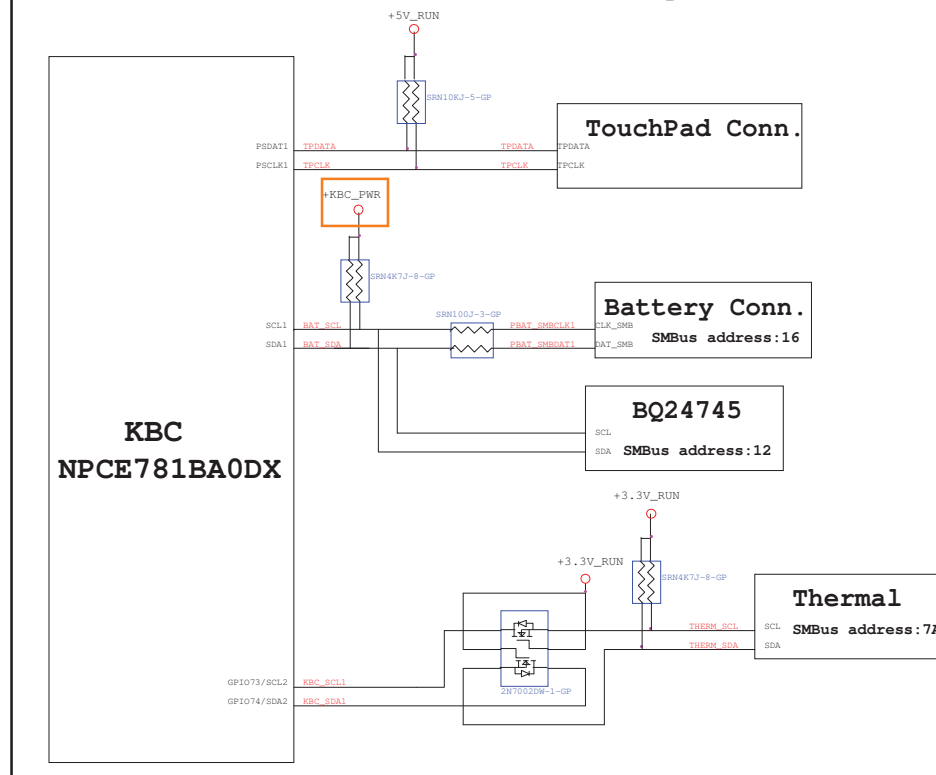
<http://hobi-elektronika.net>



# PCH SMBus Block Diagram

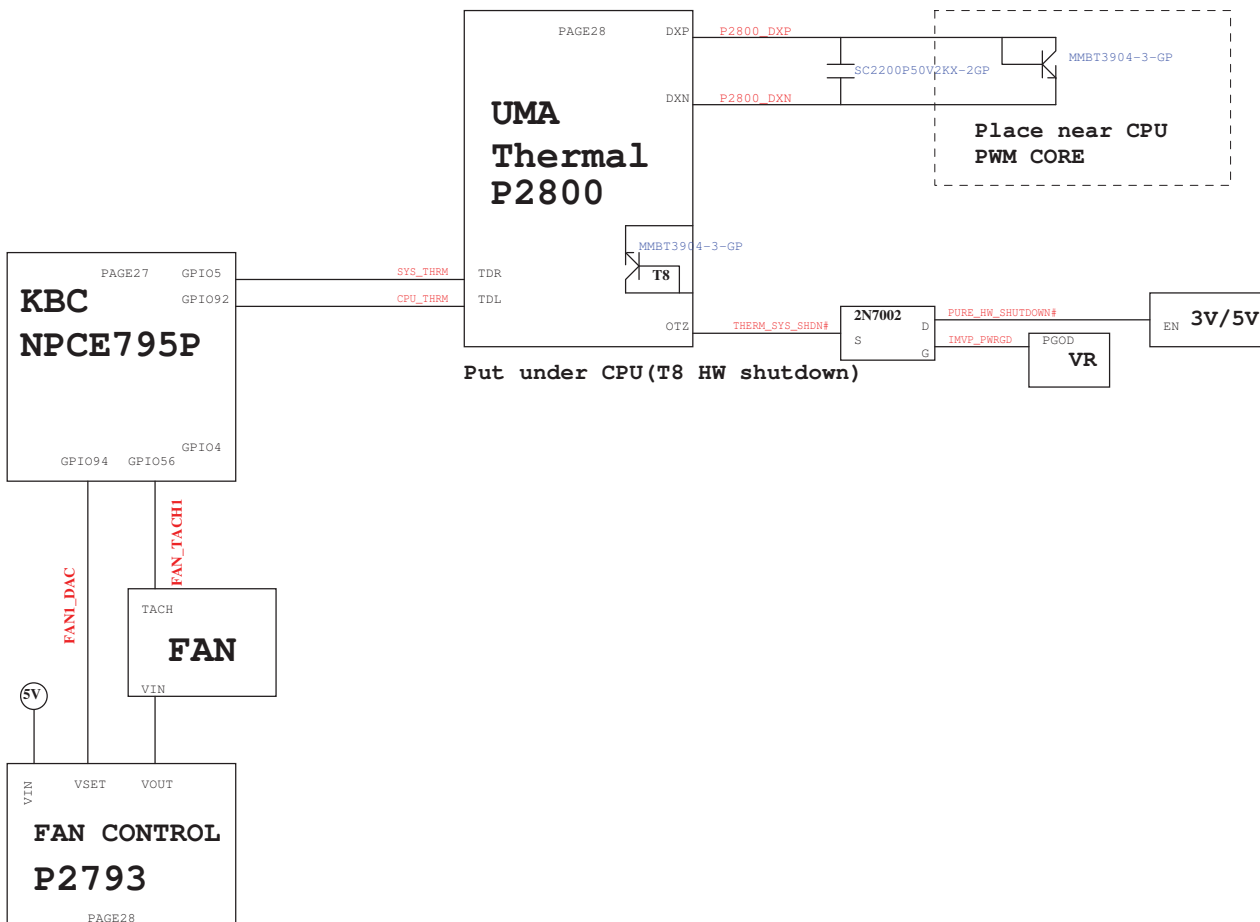


# KBC SMBus Block Diagram



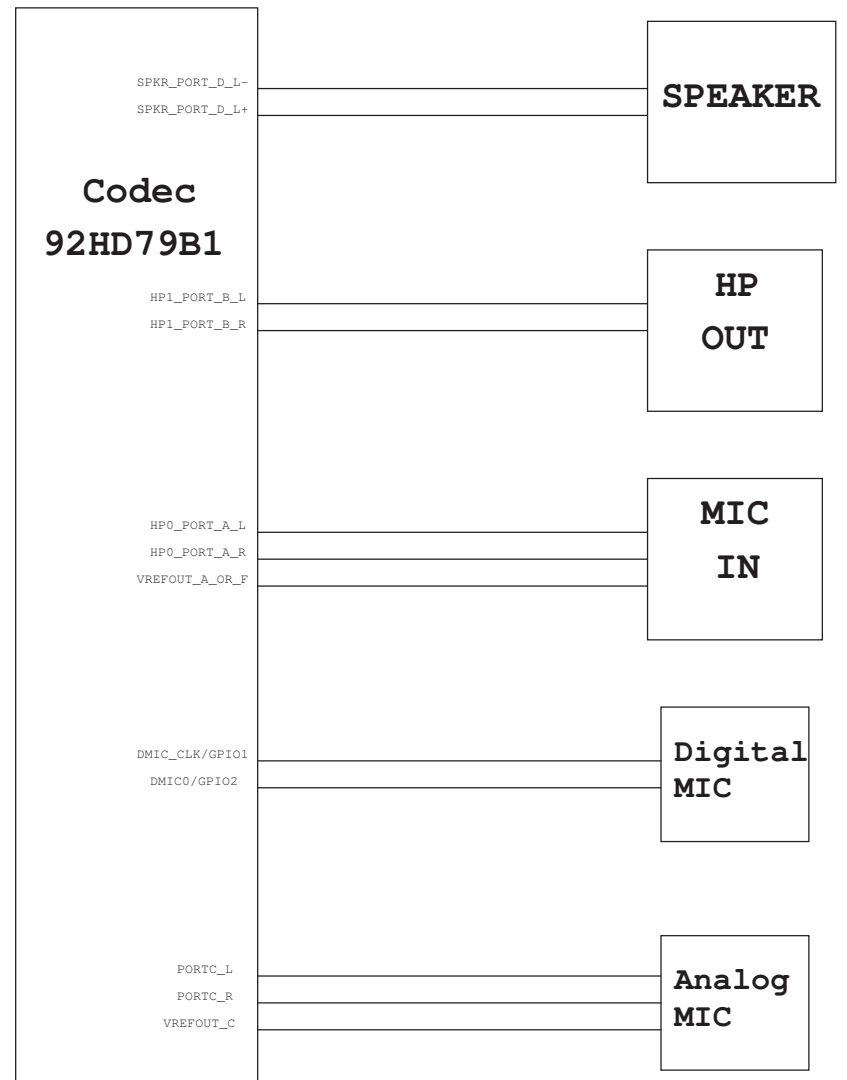
# Thermal Block Diagram

D  
C  
B  
A



<http://hobi-elektronika.net>

# Audio Block Diagram



Version	Date	Page	Function	Change Item
X01	20100818	21	EE	Sourcer suggest: Change X2101 source priority: 82.30001.A81, 82.30001.691, 82.30001.861.
X01	20100824	27	EE	Change R2724 to 20K 0402 from 10K for X01 stage.
X01	20100824	28	EE	Change U2802 Main source to 74.00991.031, 2nd 74.02793.A31,3rd 74.05606.071.
X01	20100824	28	EE	Re-assign FAN1 pin define from Niki suggestion. Pin1 : VCC;Pin2 : Ground;Pin3 : TACH.
X01	20100827	28	EE	Change FAN1 to 20.F0772.003.
X01	20100825	36	EE	Sourcer/Sarah suggest: Add U3606 2nd source 84.00460.037(VISHAY) and 3rd 84.00312.037(FAIRCHILD).
X01	20100824	40	Power	Change PR4033 to 64.20R05.16L from 64.20R05.561. Because 64.20R05.561 is Obsoleted Part.
X01	20100823	41	Power	Add LDO PU4109 for 3D3V_AUX_S5.
X01	20100824	45	Power	Change PU4501 pin7(V5IN) power source to 5V_S5 from 5V_PWR for layout routing.
X01	20100819	47	Power	Modify PR4718.1 to PWR_1D8V_FB_2.
X01	20100818	57	ME	Change ESATA1 to 22.10321.W11(with detect pin).
X01	20100824	57	EE	Change U5702 soltuion to PI5USB14550 from MAX14566.
X01	20100824	61	EE	Add 2nd 77.C1071.20L on TC6101.
X01	20100824	61	EE	Add R6101.
X01	20100824	64	EE	Re-assign FP1 pin define base on Roy updated cable connector pin define list table.
X01	20100811	65,68	EE	Add WPAN_LED# for Wifi/BT combo module.
X01	20100827	65	EE	Reserve R6508 for CLK_PCI_LPC.
X01	20100827	70	EE	Change HALLSW1 source priority: 1st: Seiko 74.05711.07B 2nd: Diodes 74.01803.07B.
X01	20100819	71	EE	Un-stuff Debug port connector(DB1) on X01.
X01	20100827	97	ME	Change H17 to ZZ.00PAD.U61
X01	20100827	97	ME	Change SPR7 to 34.42T14.002.
X01	20100827	82	EE	Modify IOBD1 pin definition: NC pin61; shift 5V_S5, 3D3V_S0, 1D5V_S0 1 pin; NC pin14.
X01	20100830	40	EE	Change PU4001 pin11 from 3D3V_AUX_S5 to 3D3V_AUX_KBC to avoid Leakage Voltage to 3D3V_AUX_KBC under DC mode.
X01	20100830	97	EMI	EMI/Simon: DY SPR1~SPR4,SPR6~SPR8.
X01	20100831	56	ME	Change ODD1 to 62.10065.221 and 2nd: 62.10065.651 to follow 20100831 connector list.
X01	20100902	22	EE	SW request: Change FFS_INT2_R to GPIO15 for ADI G-sensor. Change FFS_INT2_R to PL 1k by R2220. Remove R2201 because PCH_GPIO12 change to FFS_INT2_R.
X01	20100902	51	EE	Add 0R(R5101~R5108) for HDMI tunning.
X01	20100902	97	ME	ME suggest: Remove HBT1 Stand off(B/T).
X01	20100902	56	ME	Change ODD1 to 62.10065.651 to follow emn file.
X01	20100902	47	Power	Power/Brian: In order to assess cost down, change PL4701 to 68.2R210.20B.
X01	20100902	79	EE	U7901 G-SENSOR MAIN SOURCE change to ST(74.00351.0B3),2nd change to ADI(74.00345.0BZ)
X01	20100906	47	EE	Change PR4715 to 10K from 0ohm and stuff PC4703 for fine tune 1D8V_S0 ramp up sequence.
X01	20100906	24	EE	Add 2nd source 68.10090.10B on L2401,L2402,L2403 sync with Annie.
X01	20100906	24	EE	Add 2nd source 68.10090.10B on L2401,L2402,L2403 sync with Annie.
X01	20100906	27	EE	Add C2722 0.1uF between Q2703 G&S pin for fixed leakage voltage to 3D3V_AUX_KBC under DC mode.
X01	20100906	49	EE	Add 2nd source 74.09724.09F on U4901 sync with Annie.

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Version	Date	Page	Function	Change Item
X01	20100906	61	EE	Add 2nd source 74.00547.079 on U6I01 sync with Annie.
X01	20100906	28	EE	Updated P2800 ADJ Table from data sheet.
X01	20100906	28	EE	Change U2801,U2803 to 74.02800.A71 from 74.02800.071 from vender updated parts. Change R2803&R2817 to 107K from 499K, R2804&R2818 to 226K from 102K base on updated ADJ Table.
X01	20100906		EE	Change all of single 2N7002 to 84.2N702.J31 from 84.2N702.D31 due to 84.2N702.D31 will EOL.
X01	20100906	57	EE	Swap TR5701 for layout concern.
X01	20100906	64	EE	Change FP1 to 20.K0320.006 for emn file.
X01	20100906	64	EE	Change FP1 back to 20.K0256.006 for layout routing concern.
X01	20100907	39	EE	Change net name for BATT1 ESD diode.
X01	20100907	68	EE	Swap pin definition for PWRBTN1.
X01	20100907	4~10	EE	Update CPU1(62.10055.421) symbol.
X01	20100908	37	EE	Stuff Q3704,R3710; un-stuff R3716. U3701 pin2 change to 1.05VTT_PWRGD from RUNPWROK.
X01	20100908	22,18	EE	Change FFS_INT2_R from PCH GPIO48 to GPIO14. Keep PCH_GPIO15 PH R2201,PCH_GPIO48 PH R2220. Add R1818 10K PL on FFS_INT2_R(GPIO14).
X01	20100908	63	EE	Modify BT module to BOM option and default DY.
X01	20100909	27	EE	PSE suggest: Add AFTP2701~AFTP2703 at USB_PWR_EN#, AC_PRESENT, and E51_TxD.
X01	20100909	38	EE	PSE suggest: Add AFTP3803 at +DC_IN.
X01	20100910	41	EE	Power/Brian: PL4101 change to 68.2R210.20B. PTC4103 change to 77.22271.27L. PTC4601 change to 79.22719.20L.
X01	20100910	82	EE	Change R8201~R8203 to 62ohm from 33ohm for fine tune MEDIA_LED 5mA current.
X01	20100913	74,97	ME	Change CARD1 to 20.I0129.001 from ME/Lawrence updated latest DXF&EMN on X01. Change H11~H13 to ZZ.00PAD.V71 from ME/Lawrence updated latest DXF&EMN on X01.
X01	20100914	82	EE	Change MEDIA.1 to 5V_S5 from MEDIA_PWR. Change R8201~R8203 to 470ohm from 100ohm. Add RN8209 PH 5V_S5 on MEDIA_LED1~3# for PWM OD mode.
X01	20100914	64	EE	Re-assign FP1 pin assignment to meet the FP1 module.
X01	20100915	70	EE	Sourcer/Harrison suggests: Change HALLSW1 to 74.TCS20.03B and 74.09132.A7B.
X01	20100917	27	EE	Add Q2706 2N7002 to avoid leakage loop from 3D3V_S5 to 3D3V_AUX_KBC issue when 10mW latched fail timing. Un-stuff C2713 to follow the standard schematics.
X01	20100917	21,22	EE	Add RN2104 10K instead of R2111 10K. Move EC_SCI#,DBC_EN to RN2201. Remove RN2202. Change RN2103 to 10k array resistor to follow the standard schematics. Move S_GPIO to RN2103. Move PSW_CLR# to RN2104.
X01	20100917	27,40	Power	Rename PCIE_RST# to AD_IA_HW2 on KBC GPIO50 for power Tom suggest. Reserved PQ4004,PR4036,PR4037,PR4040 for AD_IA_HW2 function.
X01	20100917	48	Power	Change PR4809 to 4.7K from 100K PH power source change to 3D3V_S0 from S5.
X01	20100917	69	EE	Un-stuff R6907 and stuff Q6902,R6906 for 5V drive CAP_LED.
X01	20100917	82	EE	Update IOBD1 20.F1432.080 orcad symbol.
X01	20100920	56	EE	Change R5605.1 to 5V_S0.
X01	20100920	51,37	EE	Change Q5102,Q3706 main source to 84.03904.L06; 2nd to 84.03904.P11; 3rd to 84.03904.T11 from Sourcer updated.
X01	20100920	49	EE	EMI/Simon request: LVDSA_DATA0#, LVDSA_DATA0, LVDSA_DATA1#, LVDSA_DATA1,LVDSA_DATA2#,LVDSA_DATA2 add series 0 ohm resistor and grounding 10p capacitance. Add 0 ohm series 0 ohm resistors at LVDSA_CLK# and LVDSA_CLK.
X01	20100921	68	EE	Change Q6812 to PNP type for TP_LOCK_LED# is low active.
X01	20100921	19	EE	Move PCH_WAKE# to RN1901 pin3. Change R1921 to 100k ohm PH on AC_PRESENT.
X01	20100921	74	EE	Update Card1 symbol from the PDM system.
X01	20100921	82,64,21	EE	Swap MEDIA_LED3# and MEDIA_LED1#. Swap USB_PN2 and USB_PP2;BIOMETRIC_USBPIN and BIOMETRIC_USBPIN. Swap SATA_DET#0 and INT_SERIRQ.
X01	20100923	68	EE	Sync TPLOCK LED with the std schematics.
X01	20100923	37	EE	Removed R3701,C3701 and connect 0D75V_EN to U3701 pin2. Removed ID5V_S0 reserved control circuit to release layout space.
X01	20100923	5	EE	Change R504,R1812,R1813,R1815,R1817,R1903,R1906,R1924,R1925,R1910,R1912,R1913,R2213,R2219,R2711,R2733,R2761,R2807,R5125,R5721,R5722 to 0R0402 short pad from 0ohm. Change R2702 to 0 ohm 0603 short pad.

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